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RTL8685PB-CG

INTEGRATED VDSL2 ROUTER CONTROLLER WITH 5-PORT GE SWITCH

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/03/23	First release.
1.1	2018/05/11	Corrected minor typing errors.
1.2	2018/06/11	Added section 11.6 VOIP Interface, page 41.
1.3	2018/07/16	Added section 11.7 NFBI Interface Timing, page 46. Added section 11.8 VDSL PHY Bonding Interface, page 47. Corrected minor typing errors.
1.4	2018/08/17	Revised Table 39 Ordering Information, page 55. Corrected minor typing errors.
1.5	2018/10/29	Revised Table 2 Pin Assignments Table, page 13 (Pins 4, 12, 24, 35). Revised Table 39 Ordering Information, page 55.
1.6	2019/01/18	Revised Table 31 Utopia Master TX Interface Timing, page 47. Revised Table 32 Utopia Master RX Interface Timing, page 48. Revised Table 33 Utopia Slave TX Interface Timing, page 49. Revised Table 34 Utopia Slave RX Interface Timing, page 50. Corrected minor typing errors.

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1. General Description

The RTL8685PB is an integrated System-on-a-Chip (SoC) with dual CPU MIPS interAptiv™ and RLX5281, a VDSL2/ADSL2+ Discrete Multi-tone (DMT) data-pump, a PTM/ATM, hardware-based ATM Segmentation and Reassembly (SAR), a packet forwarding engine, and with USB and PCIE interfaces.

The RTL8685PB supports the MIPS interAptiv™ with clock rate up to 1GHz dual core (RTL8685PB-VA5 for 1GHz, RTL8685PB-VF5 for 750MHz) and integrates an RLX5281 processor with clock rate up to 500MHz dual core with DSP for VoIP. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU (RLX5281 and MIPS IA) testing and software development.

The RTL8685PB is designed with the Realtek RTL8275-VS (VDSL2/ADSL2+ Analog Front End) for VDSL2/ADSL2+ applications.

A built-in packet forwarding engine can perform wire-speed network traffic forwarding. The CPU may be used to handle upper layer functions, such as DHCP, HTTP, and various other protocols, and to operate with a hardware accelerated forwarding engine.

The RTL8685PB provides five physical layer transceivers for 10Base-T, 100Base-TX, and 1000Base-TX. These ports support flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 803.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability as well as enabled pause ability. It also provides an optional forced mode IEEE 802.3x full-duplex flow control and MDI/MDIX auto crossover function.

The RTL8685PB requires only a single 25MHz crystal clock input for the system, and a 3.3V and 1.1V external power supply.

The RTL8685PB supports 16550-compatible peripheral interfaces UARTs, and is provided in a TFBGA-292 package.

2. Features

CPU

- MIPS interAptiv™ 1GHz CPU
 - ◆ Two coherent MIPS32® interAptiv™ CPU cores
 - ◆ Instruction L1 Cache: 64KB, 4-way set, 32 byte line size
 - ◆ Data L1 Cache: 32KB, 4-way set, 32 byte line size
 - ◆ L2 Cache: 256KB, 8-way set, 32 byte line size
- RLX5281 500MHz CPU
 - ◆ Instruction L1 Cache: 64KB, 4-way set, 32 byte line size
 - ◆ Data L1 Cache: 32KB, 4-way set, 32 byte line size, write back policy
 - ◆ Virtually indexed, physically tagged
 - ◆ PREF instruction
 - ◆ Internal Memory
IMEM: 16KB + 16KB
DMEM: 4KB + 4KB
- Misc.
 - ◆ Power-down mode (Sleep instruction)
 - ◆ EJTAG support
 - ◆ Internal BIST
 - ◆ Internal real-time timer interrupts (Count/Compare registers)
 - ◆ 2 HW instruction breakpoint/1 HW data breakpoint.
 - ◆ Supports six hardware timers and one watchdog timer

CPU Interface (NIC)

- The NIC DMA supports multiple-descriptor-ring architecture for QoS applications

Serial NOR Flash (SPI Type)

- Supports serial and dual I/O mode for SPI Flash application
- Targeted SPI flash frequency: Up to 62.5MHz
- Flash capacity up to 16Mbyte for 3Byte address mode, and 64Mbytes for 4Byte address mode
- Boot up from SPI flash is supported

Serial NAND Flash (SPI Type)

- Supports serial, dual, and quad I/O mode for SPI Flash application
- Targeted SPI flash frequency: Up to 100MHz
- Flash capacity up to 256Mbyte
- Boot up from ROM for SPI NAND flash model is supported

Two-Chip ADSL2+/VDSL2 CPE Solution

- RTL8685PB(ADSL2+/VDSL2 Multiservice SOC)+RTL8275-VS (ADSL2+/VDSL2 Analog Front End)

DMT

- ANSI T1.413 Issue 2
- ITU-T G.992.1 (G.dmt) Annexes A and B
- G.992.2 (G.lite) Annexes A and B
- G.992.3 ADSL2 (G.dmt.bis) Annexes A, B, I, J, L, and M
- G.992.4 ADSL2 (G.lite.bis)
- G.992.5 ADSL2+
- G.993.1 VDSL
- G.993.2 VDSL2 (35b included)
- G.998.4 G.INP
- G.993.5 G.VECTOR
- Dual bearer channel dual-latency
- ATM and PTM supported.
- Embedded 'Dying-Gasp' detection circuit.

Ethernet

- Supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation and 10Base-T in full/half duplex mode
- Supports Link Down Power Saving in Ethernet PHYceivers
- Per-port configurable auto-crossover function

PCIE & USB

- PCIe 1.1 interface
- One USB 2.0 and one USB 3.0 interface integrated

3. System Applications

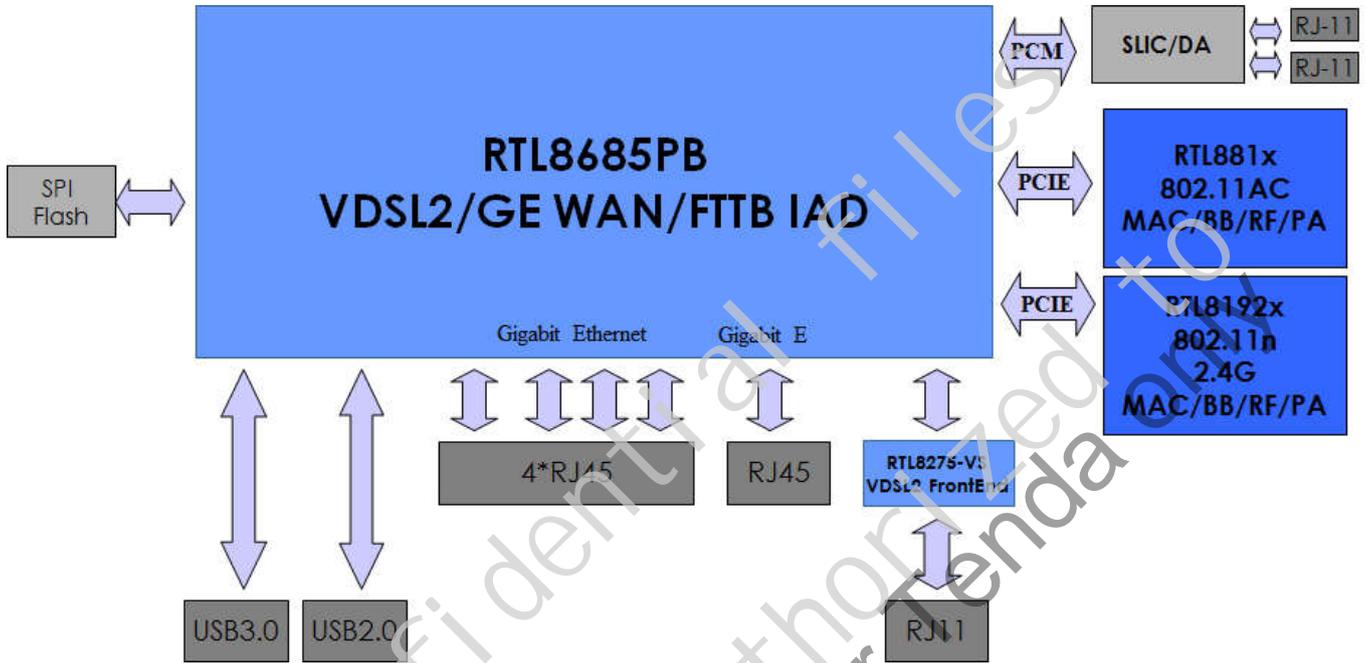


Figure 1. Typical Application Diagram

4. Block Diagram

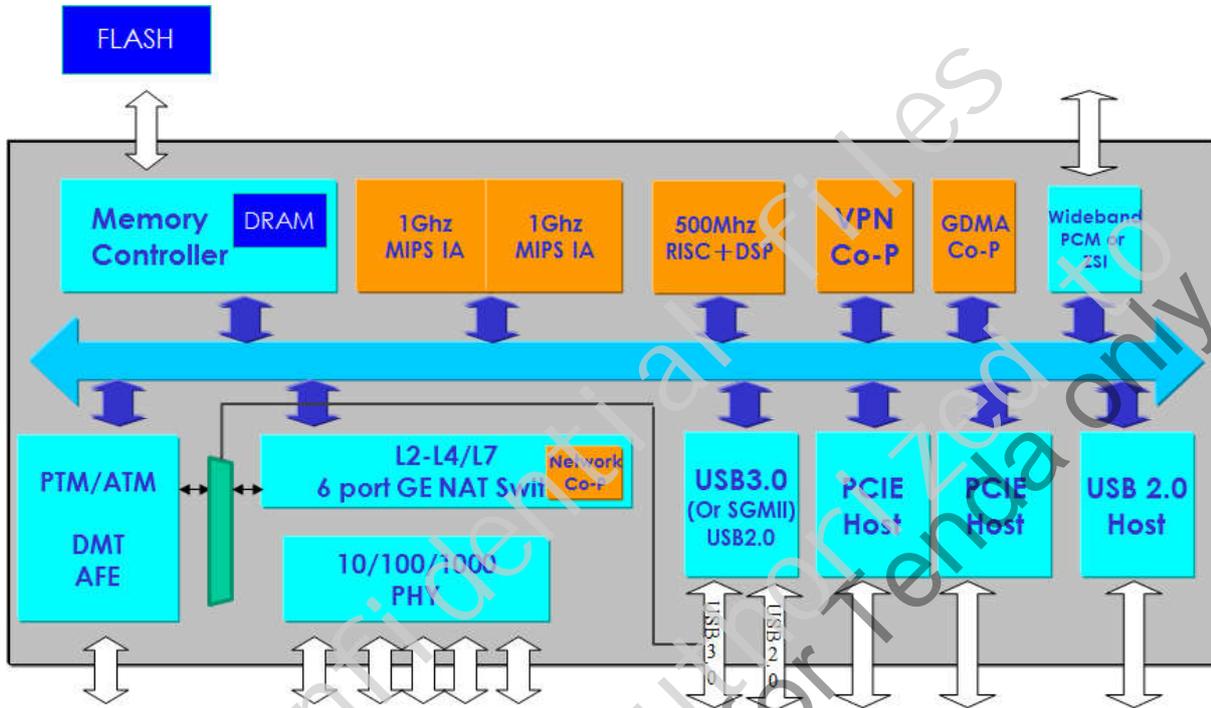


Figure 2. Block Diagram for RTL8685PB-VAx

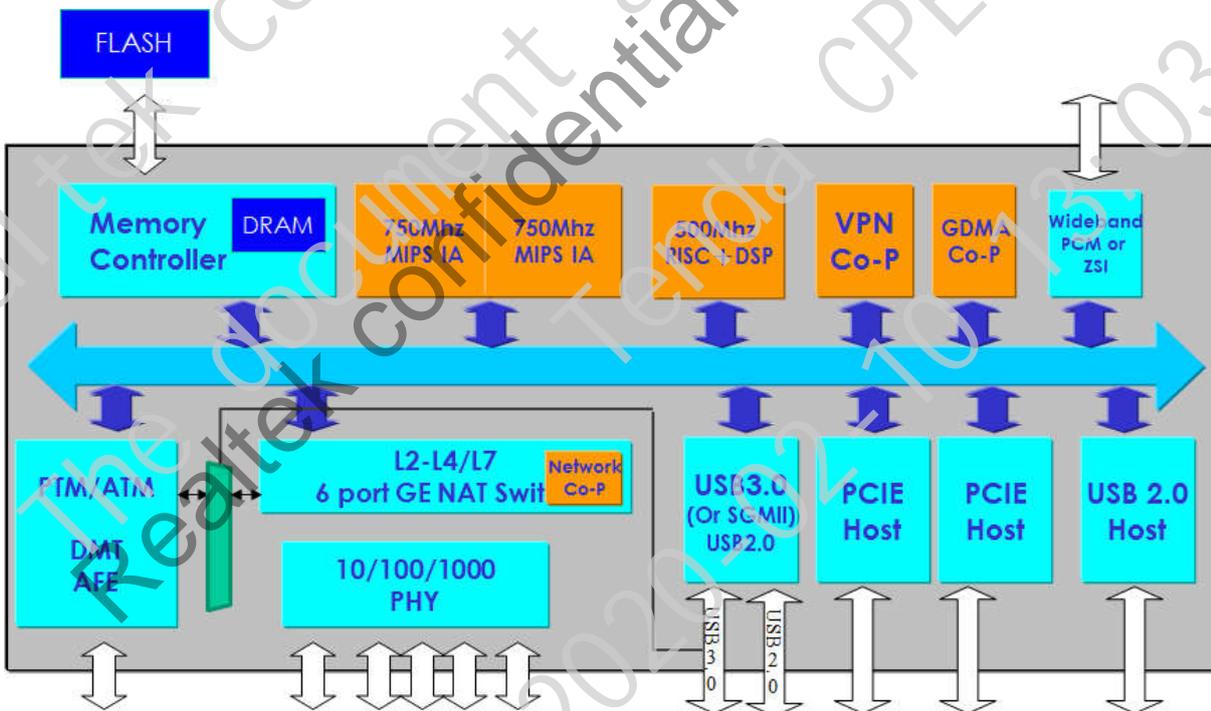


Figure 3. 750MHz Block Diagram for RTL8685PB-VFx

5. Memory Map

Table 1. Memory Map

Name	Mode	Cached	Virtual Address	Physical Address	Size	Description																	
KUSEG	Kernel User	Cached	0x0000_0000	TLB decides	2GB	RAM (spare)																	
			0x7FFF_FFFF																				
KSEG0	Kernel	Cached	0x8000_0000	0x0000_0000	256MB	System Memory																	
			0x8FFF_FFFF	0x0FFF_FFFF																			
			0x9000_0000	0x1000_0000	256MB	Same physical address space that is allocated for SFR & Boot ROM																	
			0x9FFF_FFFF	0x1FFF_FFFF																			
KSEG1	Kernel	Uncached	0xA000_0000	0x0000_0000	256MB	System Memory																	
			0xAFFF_FFFF	0x0FFF_FFFF																			
			0xB000_0000	0x1000_0000	64MB	Reserved																	
			0xB3FF_FFFF	0x13FF_FFFF																			
			0xB400_0000	0x1400_0000	64MB	Upper 60MB boot Flash space, 4MB overlap with lower																	
			0xB7FF_FFFF	0x17FF_FFFF																			
			0xB800_0000	0x1800_0000	4KB	System Register																	
			0xB800_0FFF	0x1800_0FFF																			
			0xB800_1000	0x1800_1000	512B	Memory Controller																	
			0xB800_11FF	0x1800_11FF																			
			0xB800_1200	0x1800_1200	32B	SPI Nor Flash Controller																	
			0xB800_121F	0x1800_121F																			
			Peripheral Device Space																				
									<table border="1"> <thead> <tr> <th>Base Address</th> <th>Device</th> </tr> </thead> <tbody> <tr> <td>0xB800_2000</td> <td>UART (x4)</td> </tr> <tr> <td>0xB800_3000</td> <td>Interrupt controller0</td> </tr> <tr> <td>0xB800_3100</td> <td>Reserved</td> </tr> <tr> <td>0xB800_3200</td> <td>Timer (x2)</td> </tr> <tr> <td>0xB800_3300</td> <td>PERI. GPIO Source the same GPIO pins with swcore's GPIO.</td> </tr> <tr> <td>0xB800_3400</td> <td>Reserved</td> </tr> </tbody> </table>	Base Address	Device	0xB800_2000	UART (x4)	0xB800_3000	Interrupt controller0	0xB800_3100	Reserved	0xB800_3200	Timer (x2)	0xB800_3300	PERI. GPIO Source the same GPIO pins with swcore's GPIO.	0xB800_3400	Reserved
			Base Address	Device																			
			0xB800_2000	UART (x4)																			
			0xB800_3000	Interrupt controller0																			
			0xB800_3100	Reserved																			
			0xB800_3200	Timer (x2)																			
			0xB800_3300	PERI. GPIO Source the same GPIO pins with swcore's GPIO.																			
			0xB800_3400	Reserved																			
			0xB800_3FFF						0x1800_3FFF	3KB													
			0xB800_4000						0x1800_4000														
			0xB800_4FFF						0x1800_4FFF	4KB													
0xB800_5000						0x1800_5000	4KB																
0xB800_5FFF						0x1800_5FFF																	
0xB800_6000						0x1800_6000	4KB																
0xB800_6FFF						0x1800_6FFF																	
0xB800_7000						0x1800_7000	4KB																
0xB800_7FFF						0x1800_7FFF																	

Name	Mode	Cached	Virtual Address	Physical Address	Size	Description	
			0xB800_8000	0x1800_8000	4KB	PCM	
			0xB800_8FFF	0x1800_8FFF			
			0xB800_9000	0x1800_9000	4KB	VOIP_SPI	
			0xB800_9FFF	0x1800_9FFF			
			0xB800_A000	0x1800_A000	4KB	Generic DMA engine0	
			0xB800_AFFF	0x1800_AFFF			
			0xB800_B000	0x1800_B000	2KB	VOIP Accelerator	
			0xB800_B7FF	0x1800_B7FF			
			0xB800_B800	0x1800_B800	2KB	FFT Accelerator (VOIP echo cancellation)	
			0xB800_BFFF	0x1800_BFFF			
			0xB800_C000	0x1800_C000	16KB	Reserved	
			0xB800_FFFF	0x1800_FFFF			
			0xB801_0000	0x1801_0000	8KB	Switch Cport NIC	
			0xB801_1FFF	0x1801_1FFF			
			0xB801_2000	0x1801_2000	8KB	Reserved	
			0xB801_3FFF	0x1801_3FFF			
			0xB801_4000	0x1801_4000	1KB	Reserved	
			0xB801_43FF	0x1801_43FF			
			0xB801_4400	0x1801_4400	3KB	Reserved	
			0xB801_4FFF	0x1801_4FFF			
			0xB801_5000	0x1801_5000	12KB	Reserved	
			0xB801_7FFF	0x1801_7FFF			
			0xB801_8000	0x1801_8000	4KB	Generic DMA engine1	
			0xB801_8FFF	0x1801_8FFF			
			0xB801_9000	0x1801_9000	4KB	NFBI Controller	
			0xB801_9FFF	0x1801_9FFF			
			0xB801_A000	0x1801_A000	1KB	Reserved	
			0xB801_A3FF	0x1801_A3FF			
			0xB801_A400	0x1801_A400	256B	SPI NAND flash controller	
			0xB801_A4FF	0x1801_A4FF			
			0xB801_A500	0x1801_A500	256B	Reserved	
			0xB801_A5FF	0x1801_A5FF			
			0xB801_A600	0x1801_A600	256B	FLASH ECC controller	
			0xB801_A6FF	0x1801_A6FF			
			0xB801_A700	0x1801_A700	64KB	USB Control Register	
			0xB801_FFFF	0x1801_FFFF			
			0xB802_0000	0x1802_0000			
			0xB802_FFFF	0x1802_FFFF	64KB	0xB802_1000	EHCI
						0xB802_1FFF	
						0xB802_2000	OHCI
						0xB802_2FFF	
			0xB803_0000	0x1803_0000	64KB	Reserved	
			0xB803_FFFF	0x1803_FFFF			

Name	Mode	Cached	Virtual Address	Physical Address	Size	Description
			0xB804_0000	0x1804_0000	1MB	Reserved
			0xB813_FFFF	0x1813_FFFF		
			0xB814_0000	0x1814_0000	1KB	Reserved
			0xB814_03FF	0x1814_03FF		
			0xB814_0400	0x1814_0400	3KB	Generic DMA engine2
			0xB814_0FFF	0x1814_0FFF		
			0xB814_1000	0x1814_1000	4KB	OCP-to-Lexra bridge (includes IPC registers)
			0xB814_1FFF	0x1814_1FFF		
			0xB814_2000	0x1814_2000	1688KB	Reserved
			0xB82E_7FFF	0x182E_7FFF		
			0xB82E_8000	0x182E_8000	16KB	Reserved
			0xB82E_BFFF	0x182E_BFFF		
			0xB82E_C000	0x182E_C000	16KB	Reserved
			0xB82E_FFFF	0x182E_FFFF		
			0xB82F_0000	0x182F_0000	32KB	SRAM Buffer zone (32KB)
			0xB82F_7FFF	0x182F_7FFF		
			0xB82F_8000	0x182F_8000	32KB	Reserved
			0xB82F_FFFF	0x182F_FFFF		
			0xB830_0000	0x1830_0000	16KB	SAR
			0xB830_3FFF	0x1830_3FFF		
			0xB830_4000	0x1830_4000	1008KB	Reserved
			0x183F_FFFF	0x183F_FFFF		
			0xB840_0000	0x1840_0000	32KB	PTM Fast
			0xB840_7FFF	0x1840_7FFF		
			0xB840_8000	0x1840_8000	32KB	PTM Interleave
			0xB840_FFFF	0x1840_FFFF		
			0xB841_0000	0x1841_0000	2112KB	Reserved
			0xB861_FFFF	0x1861_FFFF		
			0xB862_0000	0x1862_0000	128KB	Packet Accelerator
			0xB863_FFFF	0x1863_FFFF		
			0xB864_0000	0x1864_0000	4352KB	Reserved
			0xB8A7_FFFF	0x18A7_FFFF		
			0xB8A8_0000	0x18A8_0000	512KB	Sachem-VDSL
			0xB8AF_FFFF	0x18AF_FFFF		
			0xB8B0_0000	0x18B0_0000	512KB	PCIE0 Configuration Space

Name	Mode	Cached	Virtual Address	Physical Address	Size	Description				
			0xB8B7_FFFF	0x18B7_FFFF		0xB8B0_0000	PCIE0 DBI			
						0xB8B0_0FFF				
						0xB8B0_1000	PCIE0			
						0xB8B0_1FFF	Extended Reg			
						0xB8B1_0000	PCIE0 CFG0			
						0xB8B1_0FFF				
						0xB8B1_1000	PCIE0 CFG1			
						0xB8B1_1FFF				
						0xB8B1_2000	PCIE0 MSG			
						0xB8B1_2FFF				
						0xB8B2_0000	PCIE1 DBI			
						0xB8B2_0FFF				
						0xB8B2_1000	PCIE1			
						0xB8B2_1FFF	Extended Reg			
						0xB8B3_0000	PCIE1 CFG0			
						0xB8B3_0FFF				
						0xB8B3_1000	PCIE1 CFG1			
						0xB8B3_1FFF				
						0xB8B3_2000	PCIE1 MSG			
						0xB8B3_2FFF				
						0xB8B4_0000	-			
						0xB8B4_0FFF				
						0xB8B4_1000	-			
						0xB8B4_1FFF				
						0xB8B8_0000	0x18B8_0000	512KB	Reserved	
						0xB8BF_FFFF	0x18BF_FFFF			
						0xB8C0_0000	0x18C0_0000			
						0xB8FF_FFFF	0x18FF_FFFF	4MB	PCIE I/O space 0	
0xB8C0_0000	PCIE0 IO									
0xB8DF_FFFF										
0xB8E0_0000	PCIE1 IO									
0xB8FF_FFFF										
0xB900_0000	0x1900_0000	16MB	PCIE0 Memory Space							
0xB9FF_FFFF	0x19FF_FFFF									
0xBA00_0000	0x1A00_0000	16MB	PCIE1 Memory Space							
0xBAFF_FFFF	0x1AFF_FFFF									
0xBB00_0000	0x1B00_0000	32MB	Switch Core							
0xBCFF_FFFF	0x1CFF_FFFF									
0xBF00_0000	0x1F00_0000	12MB	Reserved							
0xBFBF_FFFF	0x1FBF_FFFF									
0xBFC0_0000	0x1FC0_0000	4MB	Lower 4MB Boot Flash space							
0xBFFF_FFFF	0x1FFF_FFFF									

Name	Mode	Cached	Virtual Address	Physical Address	Size	Description
KSEG2	Kernel	TLB decides	0xC000_0000	TLB decides	0.98GB	Reserved
			0xFF1F_FFFF	0x1FFF_FFFF		
			0xFF20_0000	0xFF20_0000	2MB	EJTAG Controller
			0xFF3F_FFFF	0xFF3F_FFFF		
			0xFF40_0000	0xFF40_0000	12MB	Reserved
			0xFFFF_FFFF	0xFFFF_FFFF		
0xFF1F_FFFF	0x1FFF_FFFF					

6. Pin Assignments

6.1. Package Identification

Green package is indicated by the 'G' in GXXX (Figure 4).



Figure 4. Package Identification

6.2. Pin Assignments Layout

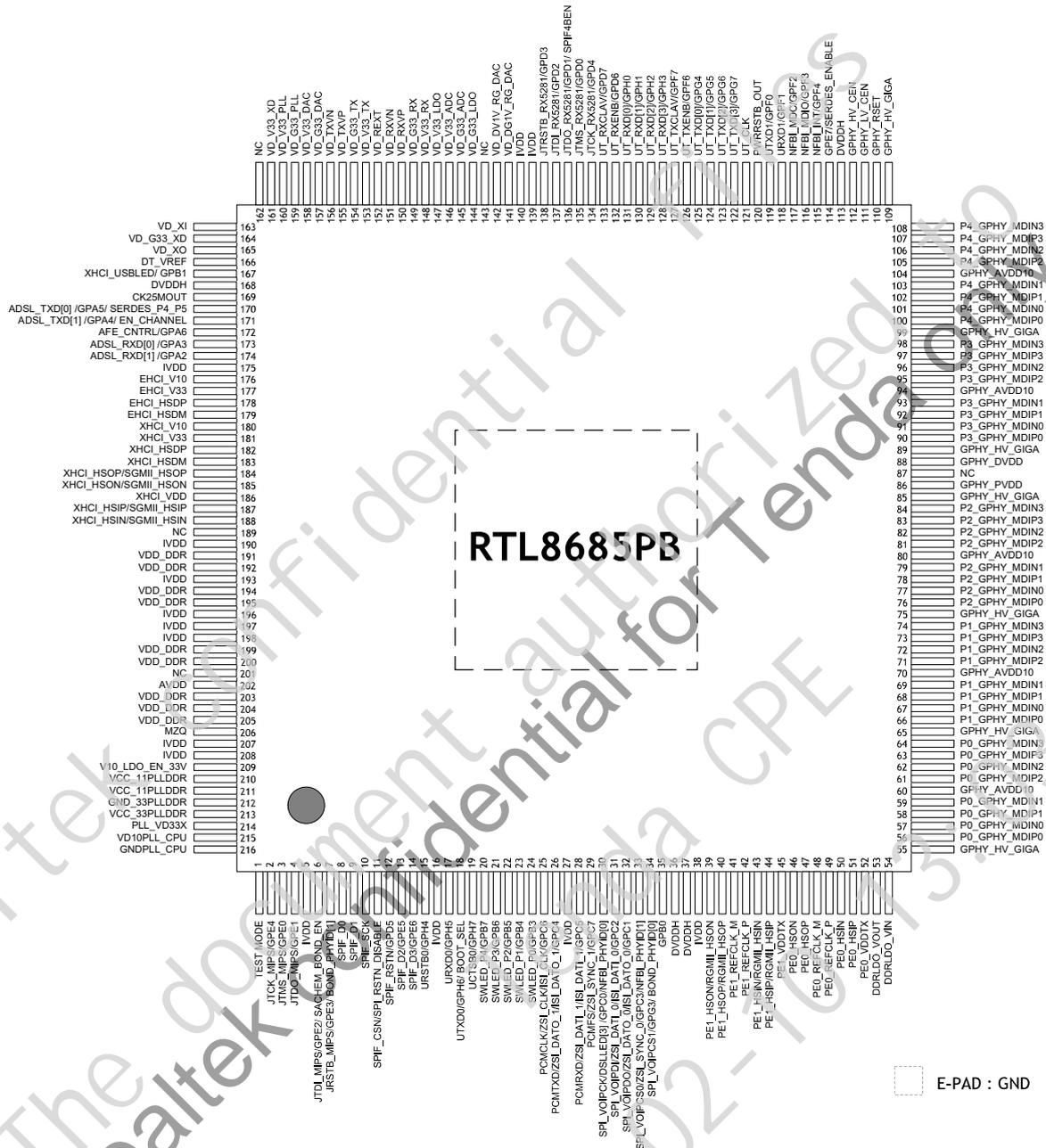


Figure 5. Pin Assignments Layout

6.3. Pin Assignments Table

The signal type codes below are used in the following tables:

- | | |
|--|--|
| I: Input Pin | AI: Analog Input Pin |
| O: Output Pin | AO: Analog Output Pin |
| I/O: Bi-Direction Input/Output Pin | AI/O: Analog Bi-Direction Input/Output Pin |
| P: Digital Power Pin | AP: Analog Power Pin |
| G: Digital Ground Pin | AG: Analog Ground Pin |
| O _{PU} : Output Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm) | O _{PD} : Output Pin With Pull-Down Resistor;
(Typical Value = 75K Ohm) |

Table 2. Pin Assignments Table

Name	Pin No.	Type	Name	Pin No.	Type
TEST MODE	1	I	IVDD	27	P
JTCK_MIPS/GPE4	2	I/O	PCMRXD/ZSI_DATI_1/ISI_DATI_1/GPC5	28	I/O
JTMS_MIPS/GPE0	3	I/O	PCMFS/ZSI_SYNC_1/GPC7	29	I/O
JTDO_MIPS/GPE1	4	O	SPI_VOIPCK/DSLLED[3]/GPC0/NFBI_PHYID[0]	30	O _{PD}
IVDD	5	P	SPI_VOIPDI/ZSI_DATI_0/ISI_DATI_0/GPC2	31	I/O
JTDI_MIPS/GPE2/SACHEM_BOND_EN	6	O _{PD}	SPI_VOIPDO/ZSI_DATO_0/ISI_DATO_0/GPC1	32	I/O
JRSTB_MIPS/GPE3/BOND_PHYID[1]	7	O _{PD}	SPI_VOIPCS0/ZSI_SYNC_0/GPC3/NFBI_PHYID[1]	33	O _{PD}
SPIF_D0	8	I/O	SPI_VOIPCS1/GPG3/BOND_PHYID[0]	34	O _{PD}
SPIF_D1	9	I/O	GPB0	35	O
SPIF_SCK	10	O	DVDDH	36	AP
SPIF_CSN/SPI_RSTN_DISABLE	11	O _{PU}	DVDDH	37	AP
SPIF_RSTN/GPD5	12	I/O	IVDD	38	P
SPIF_D2/GPE5	13	I/O	PE1_HSON/RSGMII_HSON	39	AI/O
SPIF_D3/GPE6	14	I/O	PE1_HSOP/RSGMII_HSOP	40	AI/O
URSTB0/GPH4	15	I/O	PE1_REFCLK_M	41	AI/O
IVDD	16	P	PE1_REFCLK_P	42	AI/O
URXD0/GPH5	17	I/O _{PU}	PE1_HSIN/RSGMII_HSIN	43	AI/O
UTXD0/GPH6/BOOT_SEL	18	O _{PD}	PE1_HSIP/RSGMII_HSIP	44	AI/O
UCTSB0/GPH7	19	I/O			
SWLED_P4/GPB7	20	I/O			
SWLED_P3/GPB6	21	I/O			
SWLED_P2/GPB5	22	I/O			
SWLED_P1/GPB4	23	I/O			
SWLED_P0/GPB3	24	O _{PU}			
PCMCLK/ZSI_CLK/ISI_CLK/GPC6	25	I/O			
PCMTXD/ZSI_DATO_1/ISI_DATO_1/GPC4	26	I/O			

Name	Pin No.	Type
PE1_VDDTX	45	AP
PE0_HSON	46	AI/O
PE0_HSOP	47	AI/O
PE0_REFCLK_M	48	AI/O
PE0_REFCLK_P	49	AI/O
PE0_H SIN	50	AI/O
PE0_H SIP	51	AI/O
PE0_VDDTX	52	AP
DDRLDO_VOUT	53	P
DDRLDO_VIN	54	P
GPHY_HV_GIGA	55	AP
P0_GPHY_MDIP0	56	AI/O
P0_GPHY_MDIN0	57	AI/O
P0_GPHY_MDIP1	58	AI/O
P0_GPHY_MDIN1	59	AI/O
GPHY_AVDD10	60	AP
P0_GPHY_MDIP2	61	AI/O
P0_GPHY_MDIN2	62	AI/O
P0_GPHY_MDIP3	63	AI/O
P0_GPHY_MDIN3	64	AI/O
GPHY_HV_GIGA	65	AP
P1_GPHY_MDIP0	66	AI/O
P1_GPHY_MDIN0	67	AI/O
P1_GPHY_MDIP1	68	AI/O
P1_GPHY_MDIN1	69	AI/O
GPHY_AVDD10	70	AP
P1_GPHY_MDIP2	71	AI/O
P1_GPHY_MDIN2	72	AI/O
P1_GPHY_MDIP3	73	AI/O
P1_GPHY_MDIN3	74	AI/O
GPHY_HV_GIGA	75	AP
P2_GPHY_MDIP0	76	AI/O
P2_GPHY_MDIN0	77	AI/O
P2_GPHY_MDIP1	78	AI/O
P2_GPHY_MDIN1	79	AI/O
GPHY_AVDD10	80	AP
P2_GPHY_MDIP2	81	AI/O
P2_GPHY_MDIN2	82	AI/O
P2_GPHY_MDIP3	83	AI/O
P2_GPHY_MDIN3	84	AI/O
GPHY_HV_GIGA	85	AP
GPHY_PVDD	86	AP
NC	87	-
GPHY_DVDD	88	AP

Name	Pin No.	Type
GPHY_HV_GIGA	89	AP
P3_GPHY_MDIP0	90	AI/O
P3_GPHY_MDIN0	91	AI/O
P3_GPHY_MDIP1	92	AI/O
P3_GPHY_MDIN1	93	AI/O
GPHY_AVDD10	94	AP
P3_GPHY_MDIP2	95	AI/O
P3_GPHY_MDIN2	96	AI/O
P3_GPHY_MDIP3	97	AI/O
P3_GPHY_MDIN3	98	AI/O
GPHY_HV_GIGA	99	AP
P4_GPHY_MDIP0	100	AI/O
P4_GPHY_MDIN0	101	AI/O
P4_GPHY_MDIP1	102	AI/O
P4_GPHY_MDIN1	103	AI/O
GPHY_AVDD10	104	AP
P4_GPHY_MDIP2	105	AI/O
P4_GPHY_MDIN2	106	AI/O
P4_GPHY_MDIP3	107	AI/O
P4_GPHY_MDIN3	108	AI/O
GPHY_HV_GIGA	109	AP
GPHY_RSET	110	AO
GPHY_LV_CEN	111	AP
GPHY_HV_CEN	112	AP
DVDDH	113	AP
GPE7/ SERDES ENABLE	114	O
NFBI_INT/GPF4	115	AI/O
NFBI_MDIO/GPF3	116	AI/O
NFBI_MDC/GPF2	117	AI/O
UART1_RXD/GPF1	118	I/O _{PU}
UART1_TXD/GPF0	119	I/O
PWRRSTB_OUT	120	O
UT_CLK	121	I/O
UT_TXD[3]/GPG7	122	I/O
UT_TXD[2]/GPG6	123	I/O
UT_TXD[1]/GPG5	124	I/O
UT_TXD[0]/GPG4	125	I/O
UT_TXENB/GPF6	126	I/O
UT_TXCLAV/GPF7	127	I/O
UT_RXD[3]/GPH3	128	I/O
UT_RXD[2]/GPH2	129	I/O
UT_RXD[1]/GPH1	130	I/O
UT_RXD[0]/GPH0	131	I/O

Name	Pin No.	Type
UT_RXENB/GPD6	132	I/O
UT_RXCLAV/GPD7	133	I/O
JTCK_RX5281/GPD4	134	I/O
JTMS_RX5281/GPD0	135	I/O
JTDO_RX5281/GPD1/ SPIF4BEN	136	O _{PU}
JTDI_RX5281/GPD2	137	I/O _{PD}
JTRSTB_RX5281/ GPD3	138	I/O
IVDD	139	P
IVDD	140	P
VD_DG1V_RG_DAC	141	G
VD_DV1V_RG_DAC	142	P
NC	143	-
VD_G33_LDO	144	G
VD_G33_ADC	145	AG
VD_V33_ADC	146	AP
VD_V33_LDO	147	AP
VD_V33_RX	148	AP
VD_G33_RX	149	AG
VD_RXVP	150	AI
VD_RXVN	151	AI
VD_REXT	152	AO
VD_V33_TX	153	AP
VD_G33_TX	154	AG
VD_TXVP	155	AO
VD_TXVN	156	AO
VD_G33_DAC	157	AG
VD_V33_DAC	158	AP
VD_G33_PLL	159	AG
VD_V33_PLL	160	AP
VD_V33_XD	161	AP
NC	162	-
VD_XI	163	AI
VD_G33_XD	164	P
VD_XO	165	AO
DT_VREF	166	AP
GPB1/XHCI_USBLED	167	I/O
DVDDH	168	P
CK25MOUT	169	O
ADSL_TXD[0]/GPA5/ SERDES_P4_P5	170	O _{PU}
ADSL_TXD[1]/GPA4/ EN_CHANNEL	171	O _{PD}
AFE_CNTRL/GPA6	172	I/O

Name	Pin No.	Type
ADSL_RXD[0]/GPA3	173	I/O
ADSL_RXD[1]/GPA2	174	I/O
IVDD	175	P
EHCI_V10	176	AP
EHCI_V33	177	AP
EHCI_HSDP	178	AI/O
EHCI_HSDM	179	AI/O
XHCI_V10	180	AP
XHCI_V33	181	AP
XHCI_HSDP	182	AI/O
XHCI_HSDM	183	AI/O
XHCI_HSOP/ SGMII_HSOP	184	AI/O
XHCI_HSON/ SGMII_HSON	185	AI/O
XHCI_VDD	186	AP
XHCI_HSIP/ SGMII_HSIP	187	AI/O
XHCI_HSIN/ SGMII_HSIN	188	AI/O
NC	189	-
IVDD	190	P
VDD_DDR	191	P
VDD_DDR	192	P
IVDD	193	P
VDD_DDR	194	P
VDD_DDR	195	P
IVDD	196	P
IVDD	197	P
IVDD	198	P
VDD_DDR	199	P
VDD_DDR	200	P
NC	201	-
AVDD	202	AP
VDD_DDR	203	P
VDD_DDR	204	P
VDD_DDR	205	P
MZQ	206	O
IVDD	207	P
IVDD	208	P
V10_LDO_EN_33V	209	I
VCC_11PLLDDR	210	AP
VCC_11PLLDDR	211	AP
GND_33PLLDDR	212	AG
VCC_33PLLDDR	213	AP

Name	Pin No.	Type
PLL_VD33X	214	AP
VD10PLL_CPU	215	AP
GNDPLL_CPU	216	AG

7. Pin Descriptions

Table 3. RTL8685PB (LQFP-216E) Pin Descriptions

Symbol	LQFP-216E	Type	Description
DRAM Interface			
MZQ	206	O	Reference Pin for ZQ calibration.
Gigabit Ethernet Interface			
P0_GPHY_MDIP0	56	AI/O	Gigabit Ethernet port 0, differential pair 0~3
P0_GPHY_MDIN0	57		
P0_GPHY_MDIP1	58		
P0_GPHY_MDIN1	59		
P0_GPHY_MDIP2	61		
P0_GPHY_MDIN2	62		
P0_GPHY_MDIP3	63		
P0_GPHY_MDIN3	64		
P1_GPHY_MDIP0	66	AI/O	Gigabit Ethernet port 1, differential pair 0~3
P1_GPHY_MDIN0	67		
P1_GPHY_MDIP1	68		
P1_GPHY_MDIN1	69		
P1_GPHY_MDIP2	71		
P1_GPHY_MDIN2	72		
P1_GPHY_MDIP3	73		
P1_GPHY_MDIN3	74		
P2_GPHY_MDIP0	76	AI/O	Gigabit Ethernet port 2, differential pair 0~3.
P2_GPHY_MDIN0	77		
P2_GPHY_MDIP1	78		
P2_GPHY_MDIN1	79		
P2_GPHY_MDIP2	81		
P2_GPHY_MDIN2	82		
P2_GPHY_MDIP3	83		
P2_GPHY_MDIN3	84		
P3_GPHY_MDIP0	90	AI/O	Gigabit Ethernet port 3, differential pair 0~3
P3_GPHY_MDIN0	91		
P3_GPHY_MDIP1	92		
P3_GPHY_MDIN1	93		
P3_GPHY_MDIP2	95		
P3_GPHY_MDIN2	96		
P3_GPHY_MDIP3	97		
P3_GPHY_MDIN3	98		
P4_GPHY_MDIP0	100	AI/O	Gigabit Ethernet port 4, differential pair 0~3
P4_GPHY_MDIN0	101		
P4_GPHY_MDIP1	102		
P4_GPHY_MDIN1	103		
P4_GPHY_MDIP2	105		
P4_GPHY_MDIN2	106		
P4_GPHY_MDIP3	107		
P4_GPHY_MDIN3	108		

Symbol	LQFP-216E	Type	Description
Ethernet PHY LED of Switch Ports			
SWLED [0:4]	24, 23, 22, 21, 20	O	LED driving signals for the embedded Ethernet PHYs of individual switch ports
PCIE Interface			
PE0_HSON PE0_HSOP	46 47	AO	PCIE port 0, differential data output of PCIE host
PE0_HSIN PE0_HSIP	50 51	AI	PCIE port 0, differential data input of PCIE host
PE0_REFCLK_M PE0_REFCLK_P	48 49	AO	Differential clock output of PCIE host
PE1_HSON PE1_HSOP	39 40	AO	PCIE port 1, differential data output of PCIE host
PE1_HSIN PE1_HSIP	43 44	AI	PCIE port 1, differential data input of PCIE host
PE1_REFCLK_M PE1_REFCLK_P	41 42	AO	Differential clock output of PCIE host
RSGMII Interface			
RSGMII_HSON RSGMII_HSOP	39 40	AO	RSGMII port, differential data output
RSGMII_HSIN RSGMII_HSIP	43 44	AI	RSGMII port, differential data input
USB Interface			
EHCI_HSDP EHCI_HSDM	178 179	A/I/O	USB 2.0 port 0, differential data pair
XHCI_HSDP XHCI_HSDM	182 183	A/I/O	USB 2.0 port 1, differential data pair
XHCI_HSOP XHCI_HSON	184 185	AO	USB 3.0 port, TX differential data pair
XHCI_HSIP XHCI_HSIN	187 188	AI	USB 3.0 port, RX differential data pair
SGMII Interface			
SGMII_HSOP SGMII_HSON	184 185	AO	SGMII port, TX differential data pair
SGMII_HSIP SGMII_HSIN	187 188	AI	SGMII port, RX differential data pair
AFE-D Interface			
ADSL_TXD[0:1]	170, 171	O	Digital transmit input, parallel data
ADSL_RXD[0:1]	173, 174	I	Digital receive output, parallel data;
CK25MOUT	169	O	Master clock from ADSL AFE
AFE_CNTRL	172	I/O	Control data output to ADSL AFE
AFE Interface			
VD_TXVP VD_TXVN	155 156	AO	Differential pair for analog transmit output
VD_RXVP VD_RXVN	150 151	AI	Differential pair for analog receive input

Symbol	LQFP-216E	Type	Description
JTAG Interface for RLX5281			
JTCK	134	I	JTAG test clock
JTMS	135	I	JTAG test mode select
JTDO	136	O	JTAG test data output
JTDI	137	I	JTAG test data in
JRSTB	138	I	JTAG test reset
JTAG Interface for MIPS			
JTCK_MIPS	2	I	JTAG test clock
JTMS_MIPS	3	I	JTAG test mode select
JTDO_MIPS	4	O	JTAG test data output
JTDI_MIPS	6	I	JTAG test data in
JRSTB_MIPS	7	I	JTAG test reset
VoIP Interface (PCM+SPI)			
PCMCLK	25	O	PCM Clock which Frequency is 2.048MHz
PCMTXD	26	O	PCM Transmit data
PCMRXD	28	I	PCM Receive data
PCMFS	29	O	PCM Transmit Frame Synchronization
SPI_VOIPCK	30	O	SPI Reference Clock
SPI_VOIPDI	31	I	SPI Data In
SPI_VOIPDO	32	O	SPI Data Out
SPI_VOIPCS0	33	O	SPI Chip Select Pin0
SPI_VOIPCS1	34	O _{PD}	SPI Chip Select Pin1
VoIP Interface (ZSI)			
ZSI_CLK	25	O	ZSI reference clock
ZSI_DATO_0	32	O	ZSI data out
ZSI_DATI_0	31	I	ZSI data in
ZSK_SYNC_0	33	O	ZSI frame synchronization
ZSI_DATO_1	26	O	ZSI data out
ZSI_DATI_1	28	I	ZSI data in
ZSI_SYNC_1	29	O	ZSI frame synchronization
VoIP Interface (ISI)			
ISI_CLK	25	O	ISI reference clock
ISI_DATO_0	32	O	ISI data out
ISI_DATI_0	31	I	ISI data in
ISI_DATO_1	26	O	ISI data out
ISI_DATI_1	28	I	ISI data in
UART0			
URXD0	17	I	RX data of UART 0
UTXD0	18	O	TX data of UART 0
URTSB0	15	O	Request to Send
UCTSB0	19	I	Clear to Send
UART1			
URXD1	118	I	RX data of UART 1
UTXD1	119	O	TX data of UART 1

Symbol	LQFP-216E	Type	Description
SPI FLASH			
SPIF_CS _n	11	O	Chip select
SPIF_D0	8	I/O	Serial data input for single I/O mode Serial data input & output for dual/quad I/O read mode
SPIF_D1	9	I/O	Serial data input for single I/O mode Serial data input & output for dual/quad I/O read mode
SPIF_D2	13	I/O	Serial data input & output for dual/quad I/O read mode
SPIF_D3	14	I/O	Serial data input & output for dual/quad I/O read mode
SPIF_SCK	10	O	Reference clock
SPIF_RST _n	12	O	Serial data reset pin
LDO			
LDO_EN	209	I	DDR PLL 3.3V LDO enable
Clock & Reset			
VD_XI	163	I	Crystal input of 25MHz. That supported OSC direct input.
VD_XO	165	O	Crystal output of 25MHz.
PWRRSTB_OUT	120	O	System reset output for 300ms after chip's power-on reset
NFBI			
NFBI_INT	115	I/O	MDIO Interrupt pin, Master input, Slave output.
NFBI_MDIO	116	I/O	Serial data I/O
NFBI_MDC	117	O	NFBI clock from Master to Slave.
UTOPIA			
UT_CLK	121	I/O	UTOPIA clock from Master to Slave.
UT_TXD0	125	I/O	TX data 0 (Master)
UT_TXD1	124	I/O	TX data 1 (Master)
UT_TXD2	123	I/O	TX data 2 (Master)
UT_TXD3	122	I/O	TX data 3 (Master)
UT_TXENB	126	I/O	TX data enable (Master)
UT_TXCLAV	127	I/O	TX cell available (Master)
UT_RXD0	131	I/O	RX data 0 (Master)
UT_RXD1	130	I/O	RX data 1 (Master)
UT_RXD2	129	I/O	RX data 2 (Master)
UT_RXD3	128	I/O	RX data 3 (Master)
UT_RXENB	132	I/O	RX data enable (Master)
UT_RXCLAV	133	I/O	RX cell available (Master)

Symbol	LQFP-216E	Type	Description
Power			
IVDD	5, 16, 27, 38, 139, 140, 175, 190, 193, 196, 197, 198, 207, 208	P	Digital 1.1 voltage power
GND	EPAD	G	Digital GND
PLL_VD33X	214	AP	PLL 3.3 voltage power
VD10PLL_CPU	215	AP	PLL 1.1 voltage power
GND_PLL_CPU	216	AG	PLL GND
PE0_VDDTX	52	AP	PCIE 0 1.1 voltage power
PE1_VDDTX	45	AP	PCIE 1 1.1 voltage power
GPHY_HV_GIGA	55, 65, 75, 85, 89, 99, 109	AP	GPHY 3.3 voltage power
GPHY_HV_CEN	112		
GPHY_AVDD10	60, 70, 80, 94, 104		
GPHY_LV_CEN	111	AP	GPHY 1.1 voltage power
GPHY_PVDD	86		
GPHY_DVDD	88		
VD_DV1V_RG_DAC	142	P	DAC 1.1V power
VD_DG1V_RG_DAC	141	G	DAC GND
VD_V33_TX	153		
VD_V33_RX	148		
VD_V33_PLL	160		
VD_V33_XD	161		
VD_V33_DAC	158	AP	Analog front end 3.3 voltage power
VD_V33_ADC	146		
VD_V33_LDO	147		
DVDDH	36, 37, 113, 168,		
VD_G33_TX	154		
VD_G33_RX	149		
VD_G33_PLL	159		
VD_G33_XD	164	AG	Analog frond end GND
VD_G33_DAC	157		
VD_G33_ADC	145		
VD_G33_LDO	144		
EHCI_V10 XHCI_V10	176 180	AP	USB 2.0 analog 1.1 voltage power
EHCI_V33 XHCI_V33	177 181	AP	USB 2.0 analog 3.3 voltage power
XHCI_VDD	186	AP	USB 3.0 analog 1.1V voltage power
VDD_DDR	191, 192, 194, 195, 199, 200, 203, 204, 205	P	Digital I/O supply for DRAM interface Supply 1.8V for DDR2 and 1.5V for DDR3
AVDD	202	AP	DRAM DLL 1.1 voltage power
VCC_11PLLDDR	210, 211	P	DRAM PLL 1.1 voltage power
VCC_33PLLDDR	213	P	DRAM PLL 3.3 voltage power

Symbol	LQFP-216E	Type	Description
DDRLDO_VIN	54	P	3.3V input for DDR LDO
DDRLDO_VOUT	53	P	1.1V output for DDR PLL
Misc.			
TESTMODE	1	I	Test only; leave not connected or wired to low. Pulled-down internally for normal operation
DT_VREF	166	AI	Dying Gasp voltage detect input
VD_REXT	152	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between REXT and GND.
GPHY_RSET	110	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between RSET and GND.
Strapping			
BOOT_SEL	18	I	Boot type selection 0: SPI-NOR (Default) 1: SPI-NAND Flash
SPIF4BEN	136	I	0: SPIF 4 BYTE Enable 1: SPIF 3 BYTE Enable (Default)
SACHEM_BOND_EN	6	I	0: Bond Disable (Default) 1: Bond Enable
BOND_PHYID[1] BOND_PHYID[0]	7 34	I	BOND_PHYID bit 1 (Default: 0) BOND_PHYID bit 0 (Default: 0)
NFBI_PHYID[1] NFBI_PHYID[0]	33 30	I	NFBI PHY ID bit 1 (Default: 0) NFBI PHY ID bit 0 (Default: 0)
EN_CHANNEL	171	I	Enable config channel 0: Channel Disable (Default) 1: Channel Enable
SERDES_P4_P5	170	I	Serdes stream fom P4 or P5 0: P5 1: P4 (Default)
SERDES_ENABLE	114	I	Serdes enable 1'b0: Disable serdes 1'b1: Enable serdes
SPI_RSTN_DISABLE	11	I	SPI RSTN disable 0: SPI reset Disable 1: SPI reset Enable (Default)

8. Shared I/O Mapping

Table 4. Shared I/O Pin Mapping

Pin No.	GPIO	LED/ MDC/MDIO	VOIP_IF	JTAG	UTOPIA	AFE	SPI FLASH	UART/NFBI	STRAPPING
174	GPA2	-	-	-	-	ADSL_RXD[1]	-	-	-
173	GPA3	-	-	-	-	ADSL_RXD[0]	-	-	-
171	GPA4	-	-	-	-	ADSL_TXD[1]	-	-	EN_CHANNEL
170	GPA5	-	-	-	-	ADSL_TXD[0]	-	-	SERDES_P4_P5
172	GPA6	-	-	-	-	AFE_CNTRL	-	-	-
35	GPB0	-	-	-	-	-	-	-	-
167	GPB1	XHCI USBLED	-	-	-	-	-	-	-
24	GPB3	SWLED_P0	-	-	-	-	-	-	-
23	GPB4	SWLED_P1	-	-	-	-	-	-	-
22	GPB5	SWLED_P2	-	-	-	-	-	-	-
21	GPB6	SWLED_P3	-	-	-	-	-	-	-
20	GPB7	SWLED_P4	-	-	-	-	-	-	-
30	GPC0	DSLLED[3]	SPI_VOIPCK	-	-	-	-	-	NFBI_PHYID[0]
32	GPC1	-	SPI_VOIPDO/ ZSI_DAT0_0/ ISI_DAT0_0	-	-	-	-	-	-
31	GPC2	-	SPI_VOIPDI/ ZSI_DAT1_0/ ISI_DAT1_0	-	-	-	-	-	-
33	GPC3	-	SPI_VOIPCS0 ZSI_SYNC_0	-	-	-	-	-	NFBI_PHYID[1]
26	GPC4	-	PCMTXD/ ZSI_DAT0_1/ ISI_DAT0_1	-	-	-	-	-	-
28	GPC5	-	PCMRXD/ ZSI_DAT1_1/ ISI_DAT1_1	-	-	-	-	-	-
25	GPC6	-	PCMCLK/ ZSI_CLK/ ISI_CLK	-	-	-	-	-	-
29	GPC7	-	PCMFS/ ZSI_SYNC_1	-	-	-	-	-	-
135	GPD0	-	-	JTMS_RX5281	-	-	-	-	-
136	GPD1	-	-	JTDO_RX5281	-	-	-	-	SPIF4BEN
137	GPD2	-	-	JTDI_RX5281	-	-	-	-	-
138	GPD3	-	-	JTRSTB_ RX5281	-	-	-	-	-
134	GPD4	-	-	JTCK_RX5281	-	-	-	-	-
12	GPD5	-	-	-	-	-	SPIF_RSTN	-	-
132	GPD6	-	-	-	UT_RXENB	-	-	-	-
133	GPD7	-	-	-	UT_RXCLAV	-	-	-	-
3	GPE0	-	-	JTMS_MIPS	-	-	-	-	-
4	GPE1	-	-	JTDO_MIPS	-	-	-	-	-
6	GPE2	-	-	JTDI_MIPS	-	-	-	-	SACHEM_ BOND_EN
7	GPE3	-	-	JRSTB_MIPS	-	-	-	-	BOND_ PHYID[1]
2	GPE4	-	-	JTCK_MIPS	-	-	-	-	-
13	GPE5	-	-	-	-	-	SPIF_D2	-	-
14	GPE6	-	-	-	-	-	SPIF_D3	-	-
114	GPE7	-	-	-	-	-	-	-	SERDES_ ENABLE
119	GPF0	-	-	-	-	-	-	UTXD1	-
118	GPF1	-	-	-	-	-	-	URXD0	-
117	GPF2	-	-	-	-	-	-	NFBI_MDC	-
116	GPF3	-	-	-	-	-	-	NFBI_MDIO	-
115	GPF4	-	-	-	-	-	-	NFBI_INT	-

Pin No.	GPIO	LED/ MDC/MDIO	VOIP_IF	JTAG	UTOPIA	AFE	SPI FLASH	UART/NFBI	STRAPPING
126	GPF6	-	-	-	UT_TXENB	-	-	-	-
127	GPF7	-	-	-	UT_TXCLAV	-	-	-	-
34	GPG3	-	SPI_VOIPCS1	-	-	-	-	-	BOND_PHYID[0]
125	GPG4	-	-	-	UT_TXD[0]	-	-	-	-
124	GPG5	-	-	-	UT_TXD[1]	-	-	-	-
123	GPG6	-	-	-	UT_TXD[2]	-	-	-	-
122	GPG7	-	-	-	UT_TXD[3]	-	-	-	-
131	GPH0	-	-	-	UT_RXD[0]	-	-	-	-
130	GPH1	-	-	-	UT_RXD[1]	-	-	-	-
129	GPH2	-	-	-	UT_RXD[2]	-	-	-	-
128	GPH3	-	-	-	UT_RXD[3]	-	-	-	-
15	GPH4	-	-	-	-	-	-	URSTB0	-
17	GPH5	-	-	-	-	-	-	URXD0	-
18	GPH6	-	-	-	-	-	-	UTXD0	BOOT_SEL
19	GPH7	-	-	-	-	-	-	UCTSB0	-

9. System Overview

9.1. RISC

The RTL8685PB family supports a dual-core MIPS interAptiv™ 1GHz processor and a Realtek 500MHz RISC with DSP.

The interAptiv™ multiprocessing system (MPS) is a high performance device containing two coherent processors with best-in-class power efficiency. The interAptiv architecture combines a multi-threading pipeline with a highly intelligent coherence manager to deliver best-in-class computational throughput and power efficiency. The interAptiv MPS is fully configurable and synthesizable and contain two MIPS32® interAptiv CPU cores with 32KB D-Cache and 64KB I-Cache, system-level coherence manager with L2 cache.

9.2. System Bus

The RTL8685PB family features a bus arbiter to prioritize the bus usage between the bus masters on the system bus. Each bus master may access the bus only once for each request granted. The bus arbiter is responsible for handling credit requests from each bus master. A tier-based (three-tier) round robin scheme is used to prioritize the IO modules' bus access.

9.3. Memory Controller

The RTL8685PB family memory controller supports DDR2/DDR3 interface, SPI NOR, and SPI NAND FLASH.

9.3.1. SPI Flash Controller

- SPI NAND flash frequency: Up to 100MHz
- SPI NOR flash frequency: Up to 62.5MHz
- Supports one chip
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

9.3.2. Pin Mode and Definition of Serial, Dual, and Quad I/O

Modes supported on the SPI flash interface:

Serial I/O Mode

- SPIF_SDIO0: Flash chip input pin
- SPIF_SDIO1: Flash chip output pin

Dual I/O Mode

- SPIF_SDIO0 (SI): Flash chip bi-directional pin. This is LSB
- SPIF_SDIO1 (SO): Flash chip bi-directional pin. This is MSB

Quad I/O Mode

- SPIF_SDIO 0 (SI): Flash chip bi-directional pin. This is LSB
- SPIF_SDIO 1 (SO): Flash chip bi-directional pin
- SPIF_SDIO 2 (WP#): Flash chip bi-directional pin
- SPIF_SDIO 3 (HOLD#): Flash chip bi-directional pin. This is MSB

9.4. DMT Module

The DMT (Discrete Multi-Tone) core performs DMT modulation and demodulation, Reed-Solomon coding, bit swap, interleaving, and 4D trellis coding.

- Analog Front End Interface: 2-bit TX/RX data interfaces, serial control interface
- Embedded voltage detector helps simple Dying Gasp implementation

9.5. MDI Interface

The RTL8685PB embeds five 10/100/1000M Ethernet PHYs in the chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity.

9.6. PCIE Interface

The RTL8685PB supports to attach two generic devices to its PCIE interface.

9.7. UART Module

RTL8685PB provides two generic 16550 compatible UART ports (UART0 supported hardware flow control).

9.8. GPIO Module

The RTL8685PB family has several GPIO pins. Each GPIO pin can be configured for its direction and be enabled to interrupt whenever the input logic transits. See section 7 Pin Descriptions, page 17 for availability of GPIO pins.

9.9. System Timers

Two sets of hardware timers and one watchdog timer are implemented.

- Interrupt supported

9.10. LED Control

- Ethernet NIC LED control signals
- GPIO-based LED control signals

9.11. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8685PB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the 'RESETn' signal
- Auto load the boot code and system image from flash if flash is detected.
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the CPU

10. Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 5. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
The 3.3V Power Plane, Supply Referenced to GND and AGND.	GND-0.3	+3.63	V
The 1.1V Power Plane, Supply Referenced to GND, AGND.	GND-0.3	+1.15	V

10.2. Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
Ta	Ambient Operating Temperature	-20	-	70	°C
IVDD	Digital Low Voltage Power.	1.05	1.1	1.15	V
PLL_VD33X	PLL 3.3 voltage power	3.135	3.3	3.465	V
VD10PLL_CPU	PLL 1.1 voltage power	1.05	1.1	1.15	V
PE0_VDDTX	PCIE 0 1.1 voltage power	1.05	1.1	1.15	V
PE1_VDDTX	PCIE 1 1.1 voltage power	1.05	1.1	1.15	V
GPHY_HV_GIGA GPHY_HV_CEN	GIGA Ethernet 3.3 voltage power	3.135	3.3	3.465	V
GPHY_AVDD10 GPHY_LV_CEN GPHY_PVDD GPHY_DVDD	GPHY 1.1 voltage power	1.05	1.1	1.15	V
VD_DV1V_RG_DAC	DAC/ADC 1.1V power	1.05	1.1	1.15	V
VD_V33_TX VD_V33_RX VD_V33_PLL VD_V33_XD VD_V33_DAC VD_V33_ADC VD_V33_LDO DVDDH	Analog front end 3.3 voltage power	3.135	3.3	3.465	V
V33_USB2_0 V33_USB2_1	USB 2.0 analog 3.3 voltage power	3.135	3.3	3.465	V
V10_USB2_0 V10_USB2_1	USB 2.0 analog 1.1 voltage power	1.05	1.1	1.15	V

Symbol	Parameter	Min.	Typ.	Max.	Units
USB3_VDD	USB 3.0 analog 1.1 voltage power	1.05	1.1	1.15	V
VDD_DDR	DDR3 SDRAM I/O Power Supply 1.5V DDR2 SRRAM I/O Power Supply 1.8V	1.425 1.7	1.5 1.8	1.575 1.9	V
AVDD	DRAM DLL 1.1 voltage power	1.05	1.1	1.15	V
VCC_11PLLDDR	DRAM PLL 1.1 voltage power	1.05	1.1	1.15	V
VCC_33PLLDDR	DRAM PLL 3.3 voltage power	3.135	3.3	3.465	V
DDRLDO_VIN	3.3V input for DDR LDO	3.135	3.3	3.465	V
DDRLDO_VOUT	1.5V output for DDR PLL (DDR3) 1.8V output for DDR PLL (DDR2)	1.425 1.7	1.5 1.8	1.575 1.9	V

10.3. Total Power Consumption

Table 7. Total Power Consumption

Symbol	Parameters	Condition	Consumption	Unit
V _{3V3}	Digital supply for I/O ring (3.3V)	VDSL2, Ethernet, PCIE, USB, VoIP are active	370	mA
V _{1V0}	Core power supply voltage (1.1V)		1700	mA
V _{1V5} V _{1V8}	Memory controller supply voltage (DDR2 is 1.8V, DDR3 is 1.5V)		60	mA

Note 1: If using an internal DDR LDO transfer 1.5V/1.8V from 3.3V, the V_{1V5}/V_{1V8} should be a multiple of LDO efficiency, which is 50%.

Note 2: V_{1V5}/V_{1V8} must add DRAM power consumption according to the different memory size.

10.4. Flash Bus DC Parameters

Table 8. Flash Bus DC Parameters

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V _{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V _{OH}	Output-High Voltage	-	2.4	-	-	V	3
V _{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I _{IL}	Input-Leakage Current	V _{IN} =3.3V or 0	-10	±1	10	μA	-
I _{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R _{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R _{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: V_{IH} (MAX)=V_{DDH} + 2V for a pulse width ≤ 3ns.

Note 2: V_{IL} undershoot: V_{IL} (MIN)=-2V for a pulse width ≤ 3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

10.5. USB v1.1 DC Parameters

Table 9. USB v1.1 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	-	2.0	-	-	V	2
V _{IL}	Input-Low Voltage	-	-	-	0.8	V	2
V _{OH}	Output-High Voltage	-	2.4	-	-	V	2
V _{OL}	Output-Low Voltage	-	-	-	0.4	V	2
I _{IL}	Input-Leakage Current	V _{IN} =3.3V or 0	-	-	-	μA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

Note 2: For additional information, see the USB v1.1 Specification.

10.6. USB v2.0 DC Parameters

Table 10. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	-	200	-	-	mV	2
V _{IL}	Input-Low Voltage	-	-	-	10	mV	2
V _{OH}	Output-High Voltage	-	300	-	500	mV	2
V _{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I _{IL}	Input-Leakage Current	-	-	-	-	μA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

Note 2: For additional information, see the USB v2.0 Specification.

10.7. USB v3.0 DC Parameters

Table 11. USB v3.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{TX-DIFF-PP}	Differential Output Voltage	-	800	-	1200	mV	-
V _{RX-LFPS-DET-DIF-FP-P}	Differential Input-Low Voltage	-	100	-	300	mV	-

Note 1: These values are typical values checked in the manufacturing process and are not tested.

Note 2: For additional information, see the USB v3.0 Specification.

10.8. UART DC Parameters

Table 12. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V _{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V _{OH}	Output-High Voltage	-	2.4	-	-	V	1
V _{OL}	Output-Low Voltage	-	-	-	0.4	V	1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
I _{IL}	Input-Leakage Current	V _{IN} =3.3V or 0	-10	±1	10	μA	2
R _{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R _{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for UART related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.9. GPIO DC Parameters

Table 13. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V _{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V _{OH}	Output-High Voltage	-	2.4	-	-	V	1
V _{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I _{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R _{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GPIO related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.10. JTAG DC Parameters

Table 14. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V _{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V _{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V _{OH}	Output-High Voltage	I _{OH} =2~16mA	2.4	-	-	V	1
V _{OL}	Output-Low Voltage	I _{OL} =2~16mA	-	-	0.4	V	1
I _{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R _{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

10.11. VREF Input

Table 15. VREF Input

Symbol	Parameter	Min.	Typ.	Max.	Units
Vtrigger	Dying gasp trigger level (high to low)	-	1.16	-	V
Vtrigger	Dying gasp trigger level (low to high)	-	1.16	-	V

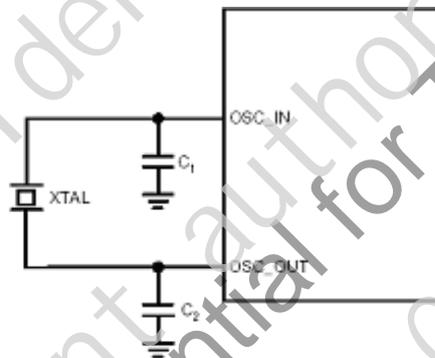
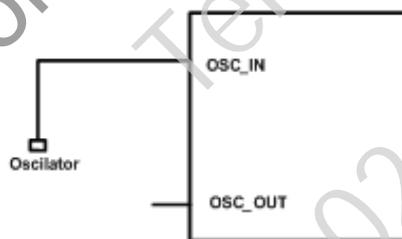
11. AC Characteristics

11.1. 25MHz System Clock Timing

Table 16. 25MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	878	-	-	mV	-
V_{IL}	Input-Low Voltage	-	-	278	mV	-
$T_{FREQUENCY}$	Clock Frequency for RTL8685PB Crystal or Oscillator	-	25	-	MHz	1
$\Delta_{FREQUENCY}$	Clock Tolerance Over 0°C to 50°C	-50	-	50	ppm	-
C_{SHUNT}	Crystal Parameter (Sometimes Referred to as the Holder Capacitance)	-	-	7	pF	-
T_{DC}	Duty Cycle	40	50	60	%	-

Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

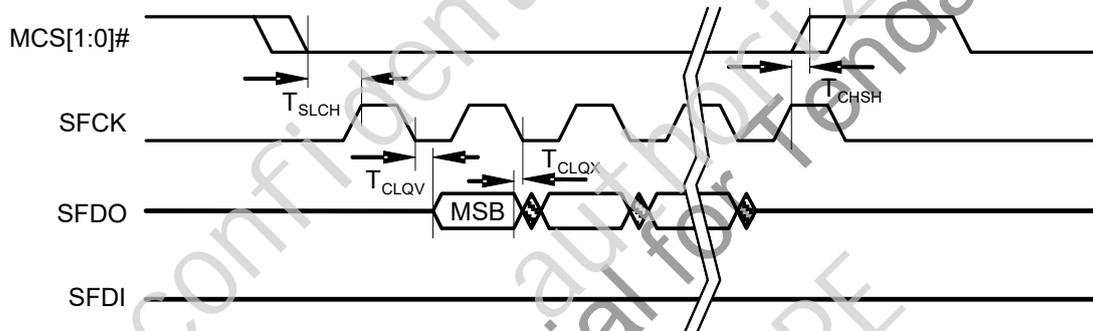

Figure 6. Typical Connection to a Crystal

Figure 7. Typical Connection to an Oscillator

11.2. Serial Flash Interface

11.2.1. Serial Flash Interface Output Timing

Table 17. Serial Flash Interface Output Timing

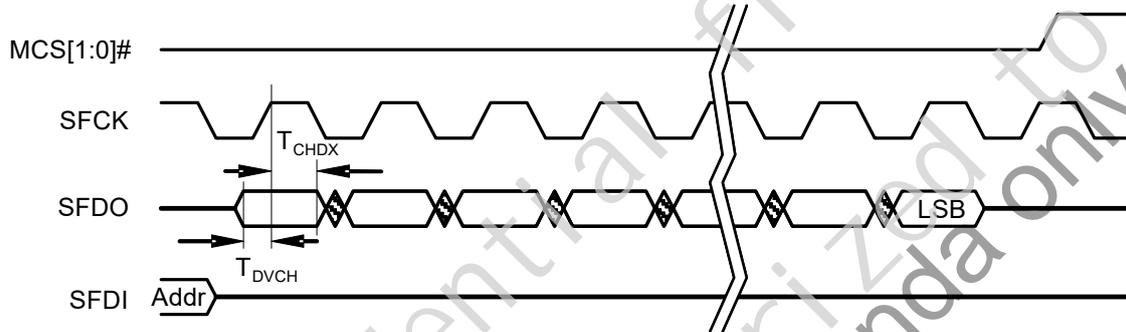
Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SLCH}	The Timing Interval from Chip-Select Activated to the First Clock Rising Edge	$0.5 * T_{SFCK} - 1$	-	$0.5 * T_{SFCK}$	ns
T_{CHSH}	The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated	$T_{SFCK} + 7$	-	$T_{SFCK} + 9$	ns
T_{CLQV}	The Timing Interval from the Last Clock Falling Edge to Data-Out Validated	-	-	1	ns
T_{CLQX}	The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated	-1	-	-	ns


Figure 8. Serial Flash Interface Output Timing

11.2.2. Serial Flash Interface Input Timing

Table 18. Serial Flash Interface Input Timing

Symbol	Parameter	Min.	Typ	Max	Units
T_{DVCH}	The Timing Interval from Data-Input Ready to the Clock Rising Edge	0	-	-	ns
T_{CHDX}	The Timing Interval from the Clock Rising Edge to Data-Input Invalidated	$0.5 * T_{SFCK}$	-	-	ns


Figure 9. Serial Flash Interface Input Timing

11.3. AFE Interface Clock

Table 19. AFE Interface Clock

Symbol	Parameter	Typ.	Unit	Notes
F	Clock frequency	75 37.5	MHz	-
Tper	Clock period	13.3 26.7	ns	-
Th	Clock duty cycle	50	%	-

Note 1: AFE RX I/F and RX I/F

RX1/RX0 and CLKM are asynchronous. RX1 and RX0 do not have a timing specification.

Note 2: AFE TX I/F and RX I/F

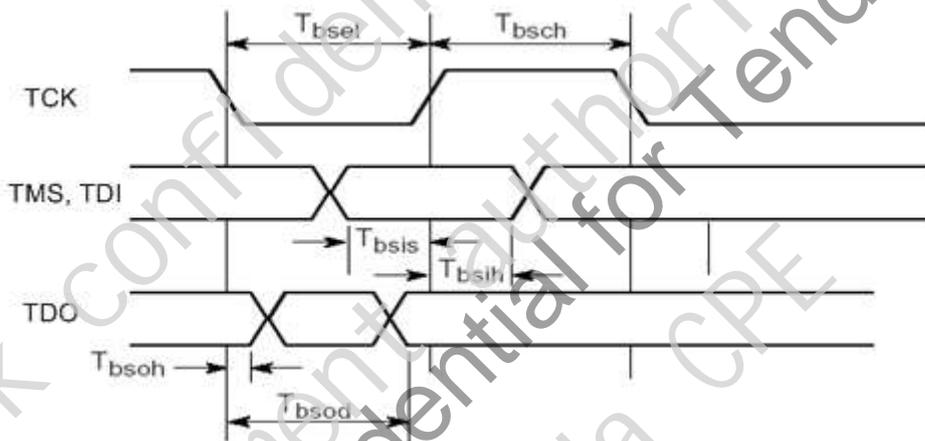
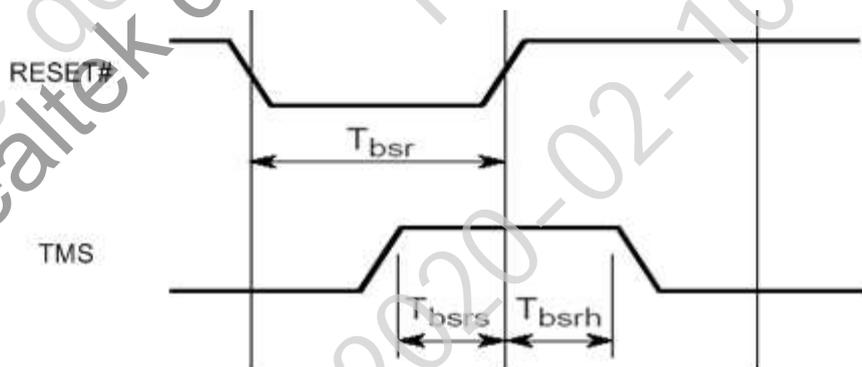
TX1/TX0 and CLKM are asynchronous. TX1 and TX0 do not have a timing specification.

11.4. JTAG Boundary Scan

Table 20. JTAG Boundary Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTAG Clock Low Time	50	-	-	ns	1
T_{bsch}	JTAG Clock High Time	50	-	-	ns	1
T_{bsis}	TDI, TMS Setup Time to Rising Edge of TCK	10	-	-	ns	-
T_{bsih}	TDI, TMS Hold Time from Rising Edge of TCK	10	-	-	ns	-
T_{bsoh}	TDO Hold Time after Falling Edge of TCK	1.5	-	-	ns	-
T_{bsod}	TDO Output from Falling Edge of TCK	-	-	40	ns	-
T_{bsr}	JTAG Reset Period	30	-	-	ns	-
T_{bsrs}	TMS Setup Time to Rising Edge of JTAG Reset	10	-	-	ns	-
T_{bsrh}	TMS Hold Time from Rising Edge of JTAG Reset	10	-	-	ns	-

Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.


Figure 10. Boundary-Scan General Timing

Figure 11. Boundary-Scan Reset Timing

11.5. PCI Express Bus Parameters

11.5.1. Differential Transmitter Parameters

Table 21. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
V _{TX-DIFFp-p}	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
V _{TX-DE-RATIO}	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
TTX-EYE	Minimum Tx Eye Width	0.75	-	-	UI
T _{TX-EYE-MEDIAN-to-MAX-JITTER}	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
T _{TX-RISE, TX-FALL}	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
V _{TX-CM-ACp}	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
V _{TX-CM-DCACTIVE-IDLEDELTA}	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
V _{TX-CM-DCLINE-DELTA}	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
V _{TX-IDLE-DIFFp}	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
V _{TX-RCV-DETECT}	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
V _{TX-DC-CM}	Tx DC Common Mode Voltage	0	-	3.6	V
I _{TX-SHORT}	Tx Short Circuit Current Limit	-	-	90	mA
T _{TX-IDLE-MIN}	Minimum Time Spent in Electrical Idle	50	-	-	UI
T _{TX-IDLE-SETTO-IDLE}	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
T _{TX-IDLE-TOTO-DIFF-DATA}	Maximum Time to Transition to Valid Tx Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
RL _{TX-DIFF}	Differential Return Loss	10	-	-	dB
RL _{TX-CM}	Common Mode Return Loss	6	-	-	dB
Z _{TX-DIFF-DC}	DC Differential Tx Impedance	80	100	120	Ω
L _{TX-SKEW}	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C _{TX}	AC Coupling Capacitor	75	-	200	nF
T _{crosslink}	Crosslink Random Timeout	0	-	1	ms

Note 1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note 2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz ~ 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

11.5.2. Differential Receiver Parameters

Table 22. Differential Receiver Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

11.5.3. REFCLK Parameters

Table 23. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to $+150\text{mV}$ on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See

Figure 15, page 39.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 12, page 38.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 12, page 38.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 14, page 39.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 12, page 38.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 12, page 38.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 12, page 38.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 18, page 40. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load $CL=2\text{pF}$.

Note12: TSTABLE is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to droop back into the $VRB \pm 100\text{mV}$ differential range. See Figure 17, page 40.

Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is $1/1,000,000$ th of 100.000000MHz exactly, or 100Hz . For 300ppm then we have an error budget of $100\text{Hz/ppm} * 300\text{ppm} = 30\text{kHz}$. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The $\pm 300\text{ppm}$ applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of $+2800\text{ppm}$.

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a $\pm 75\text{mV}$ window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 13, page 39.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

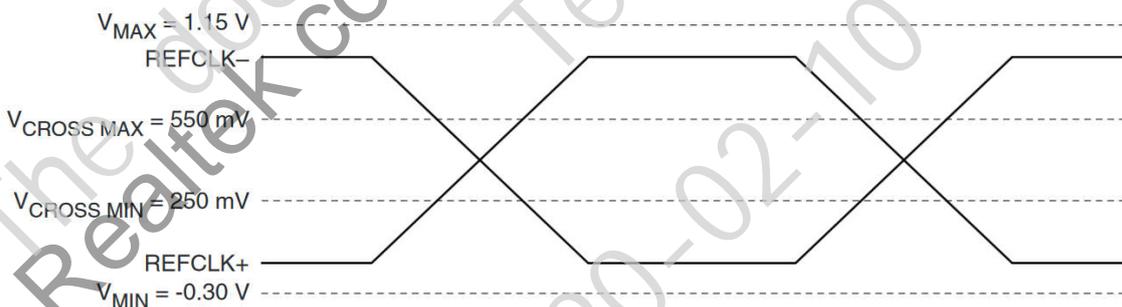


Figure 12. Single-Ended Measurement Points for Absolute Cross Point and Swing

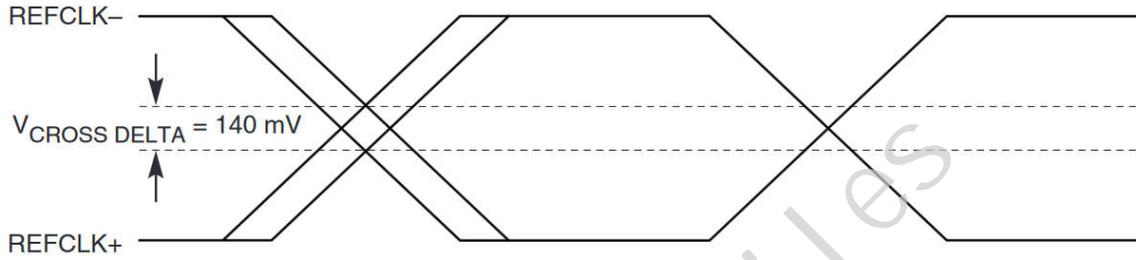


Figure 13. Single-Ended Measurement Points for Delta Cross Point

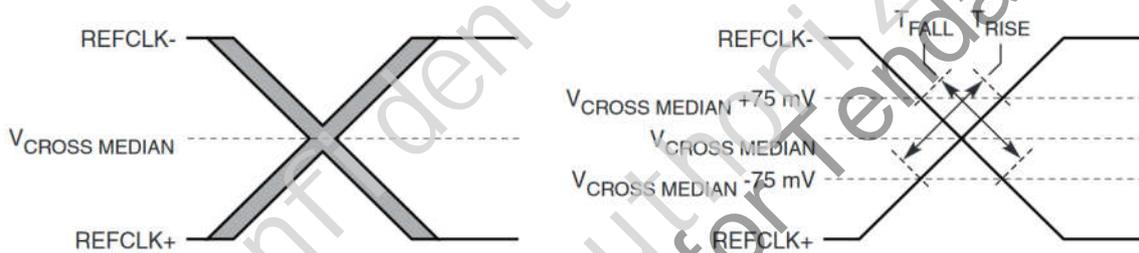


Figure 14. Single-Ended Measurement Points for Rise and Fall Time Matching

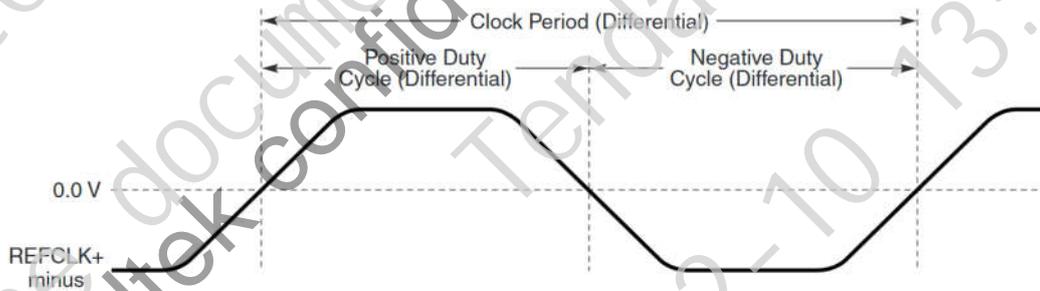


Figure 15. Differential Measurement Points for Duty Cycle and Period



Figure 16. Differential Measurement Points for Rise and Fall Time

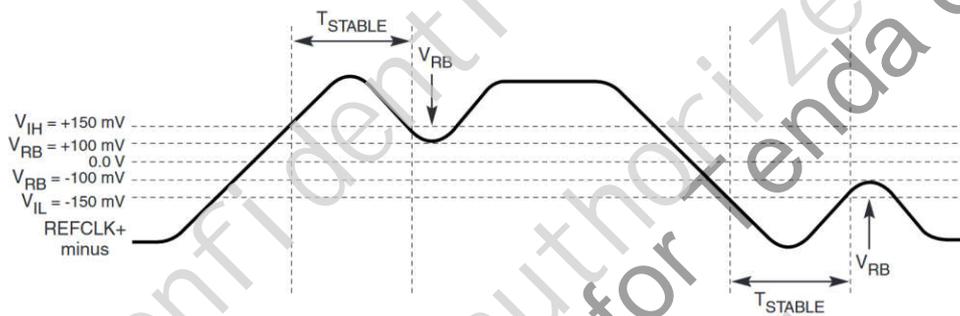


Figure 17. Differential Measurement Points for Ringback

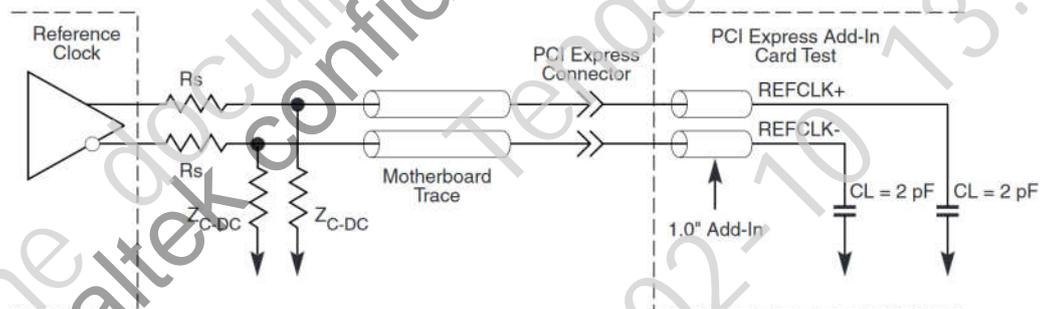


Figure 18. Reference Clock System Measurement Point and Loading

11.6. VOIP Interface

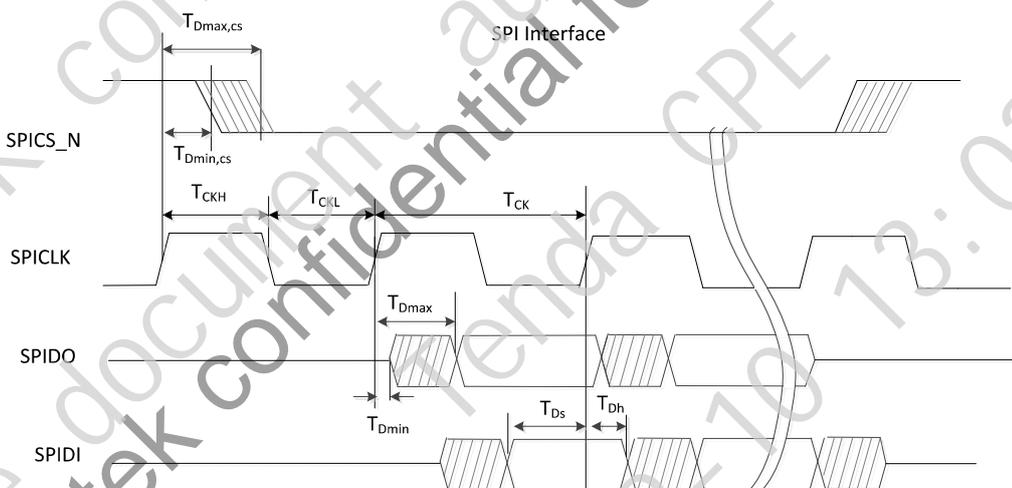
11.6.1. VOIP SPI Interface Timing

Table 24. VOIP SPI Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	SPICLK Period	64	-	-	ns	-
T_{CKL}	PCLK High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	PCLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
$T_{Dmax,cs}$	SPICS_N[1:0] max output time from SPICLK rising	-	-	32.8	ns	-
$T_{Dmin,cs}$	SPICS_N[1:0] min output time from SPICLK rising	24.4	-	-	ns	-
T_{Dmax}	SPIDO output max delay from SPICLK rising	-	-	32.8	ns	-
T_{Dmin}	SPIDO output min delay from SPICLK rising	24.4	-	-	ns	-
T_{Ds}	SPIDI input setup time to SPICLK rising	8.73	-	-	ns	-
T_{Dh}	SPIDI input hold time from SPICLK rising	-2.9	-	-	ns	-

Note 1: Input signal: SPIDI.

Note 2: Output signals: SPICLK, SPICS_N[1:0], SPIDO.


Figure 19. VOIP SPI Interface Input and Output Timing

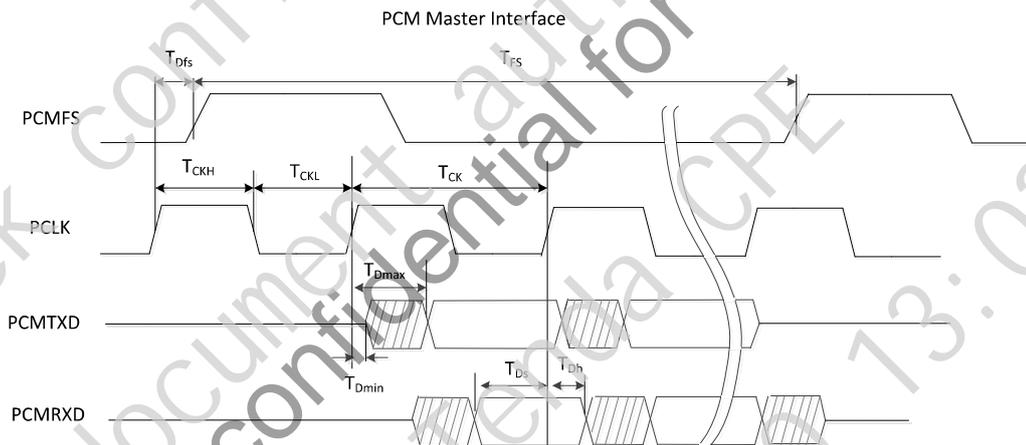
11.6.2. PCM Master Interface Timing

Table 25. PCM Master Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	PCLK Period	122	-	-	ns	Up to 8.192MHz
T_{CKL}	PCLK High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	PCLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{FS}	PCMFS Period	-	125	-	μ s	8kHz
T_{Dfs}	PCMFS output delay from PCLK rising	41	-	49	ns	-
T_{Dmax}	PCMTXD output max delay from PCLK rising	-	-	6.4	ns	-
T_{Dmin}	PCMTXD output min delay from PCLK rising	-0.2	-	-	ns	-
T_{Ds}	PCMRXD input setup time to PCLK rising	11.6	-	-	ns	-
T_{Dh}	PCMRXD input hold time from PCLK rising	-3.5	-	-	ns	-

Note 1: PCMRXD is connected to DXA, and PCMTXD is connected to the DRA pin of external SLIC.

Note 2: PCK and PCMFS are output signals.

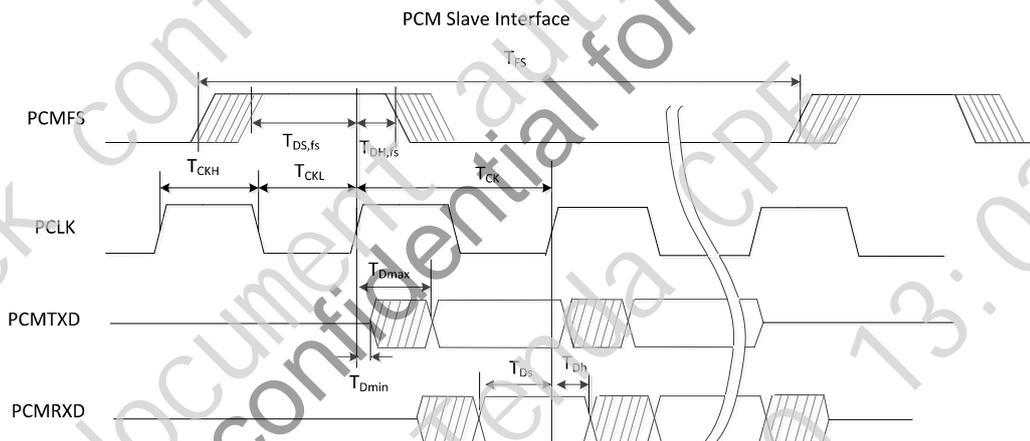

Figure 20. PCM Master Interface Input and Output Timing

11.6.3. PCM Slave Interface Timing

Table 26. PCM Slave Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	PCLK Period	480	-	-	ns	Up to 2.048MHz
T_{CKL}	PCLK High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	PCLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{FS}	PCMFS Period	-	125	-	μ s	8kHz
$T_{DS,fs}$	PCMFS input setup time to PCLK rising	10	-	-	ns	-
$T_{DH,fs}$	PCMFS input hold time from PCLK rising	1.0	-	-	ns	-
T_{Ds}	PCMRXD input setup time to PCLK rising	3	-	-	ns	-
T_{Dh}	PCMRXD input hold time from PCLK rising	2.2	-	-	ns	-
T_{Dmax}	PCMTXD output max delay from PCLK rising	-	-	15.8	ns	-
T_{Dmin}	PCMTXD output min delay from PCLK rising	4.4	-	-	ns	-

Note: PCK and PCMFS are input signals.


Figure 21. PCM Slave Interface Input and Output Timing

11.6.4. ZSI Interface Timing

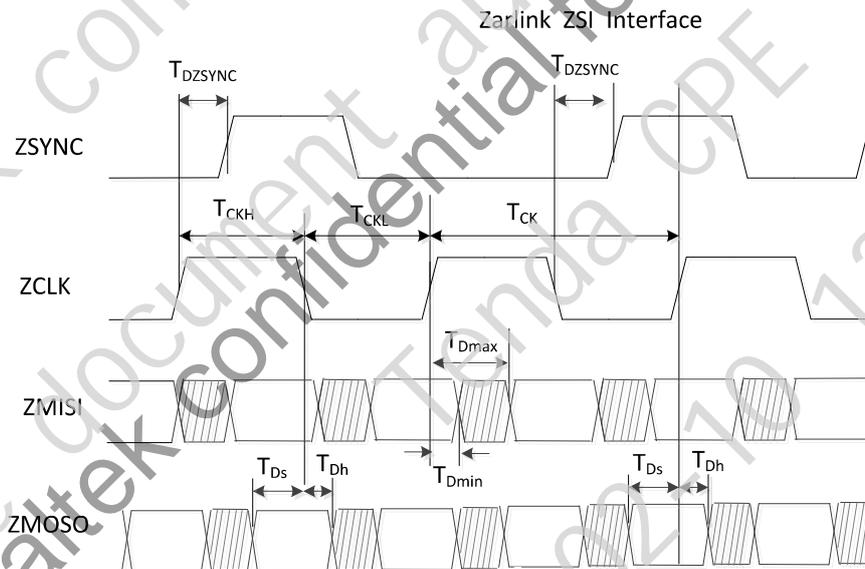
Table 27. ZSI Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	ZCLK Period	122	-	-	ns	Up to 8.196MHz
T_{CKL}	ZCLK High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	ZCLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{DZSYNC}	ZSYNC[1:0] output time from SPICLK rising or falling	40.5	-	48	ns	-
T_{Dmax}	ZMISI[1:0] output max delay from ZCLK rising or falling	-	-	48	ns	-
T_{Dmin}	ZMISI[1:0] output min delay from ZCLK rising or falling	40.5	-	-	ns	-
T_{Ds}	ZMOSO[1:0] input setup time to ZCLK rising and falling	10.1	-	-	ns	-
T_{Dh}	ZMOSO[1:0] input hold time from ZCLK rising and falling	-3.2	-	-	ns	-

Note 1: Input signal: ZMOSO[1:0].

Note 2: Output signals: ZCLK, ZSYNC[1:0], ZMISI[1:0].

Note 3: This is a double-edged interface.


Figure 22. ZSI Interface Input and Output Timing

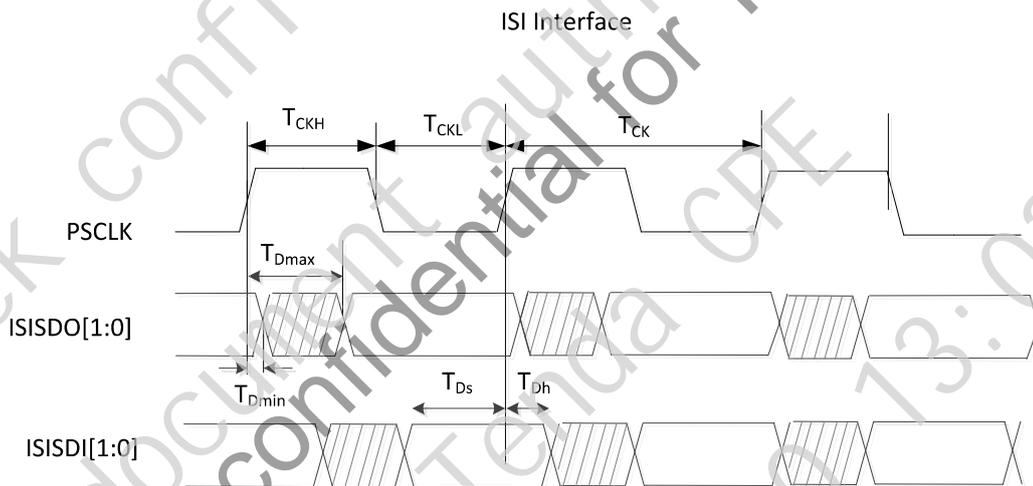
11.6.5. ISI Interface Timing

Table 28. ISI Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	PSCLK Period	40.69	-	-	ns	Up to 24.576MHz
T_{CKL}	PSCLK High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	PSCLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{Dmax}	ISISDO[1:0] output max delay from PSCLK rising	-	-	5.9	ns	-
T_{Dmin}	ISISDO[1:0] output min delay from PSCLK rising	0.6	-	-	ns	-
T_{Ds}	ISISDI[1:0] input setup time to PSCLK rising	11.7	-	-	ns	-
T_{Dh}	ISISDI[1:0] input hold time from PSCLK rising	-3.4	-	-	ns	-

Note 1: Input signal: ISISDI[1:0].

Note 2: Output signals: PSCLK, ISISDO[1:0].


Figure 23. ISI Interface Input and Output Timing

11.7. NFBI Interface Timing

11.7.1. NFBI Master Interface Timing

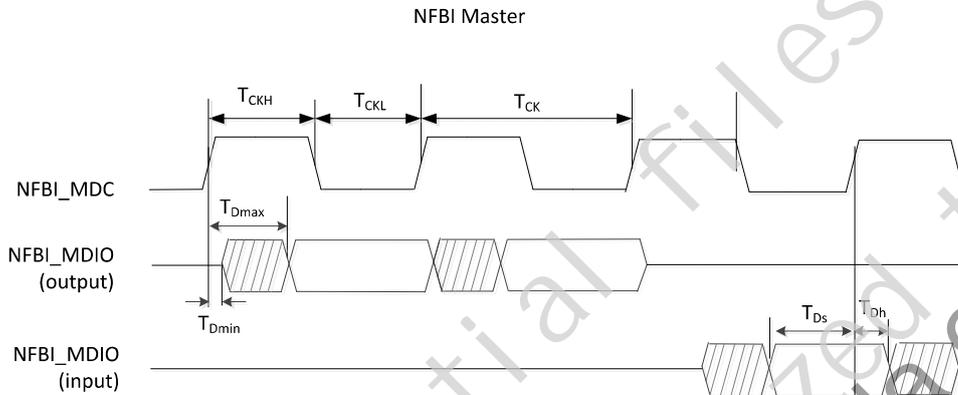


Figure 24. NFBI Master Interface Input and Output Timing

Table 29. NFBI Master Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	NFBI MDC Period	-	40	-	ns	1
T_{CKL}	MDC High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	MDC Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{Dmax}	MDIO output max delay from MDC rising	-	-	5.2	ns	-
T_{Dmin}	MDIO output min delay from MDC rising	0.7	-	-	ns	-
T_{Ds}	MDIO input setup time to MDC rising	4.4	-	-	ns	-
T_{Dh}	MDIO input hold time from MDC rising	-0.6	-	-	ns	-

Note 1: MDC is an output signal.

11.7.2. NFBI Slave Interface Timing

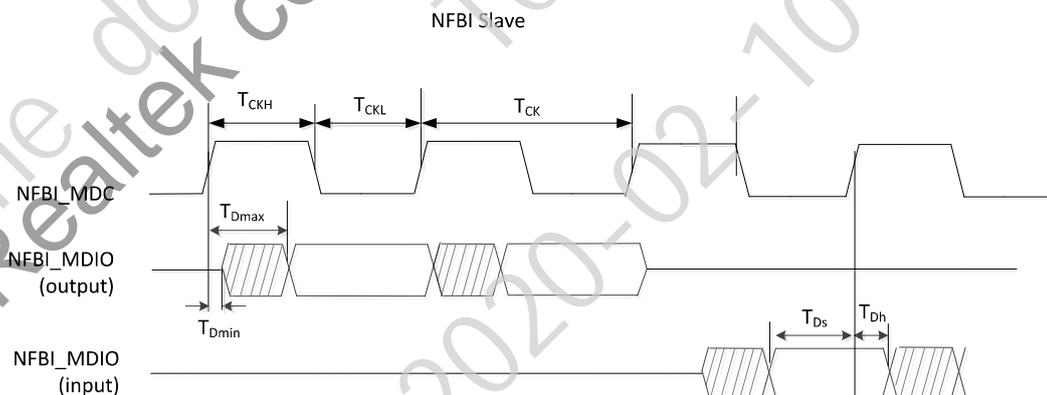


Figure 25. NFBI Slave Interface Input and Output Timing

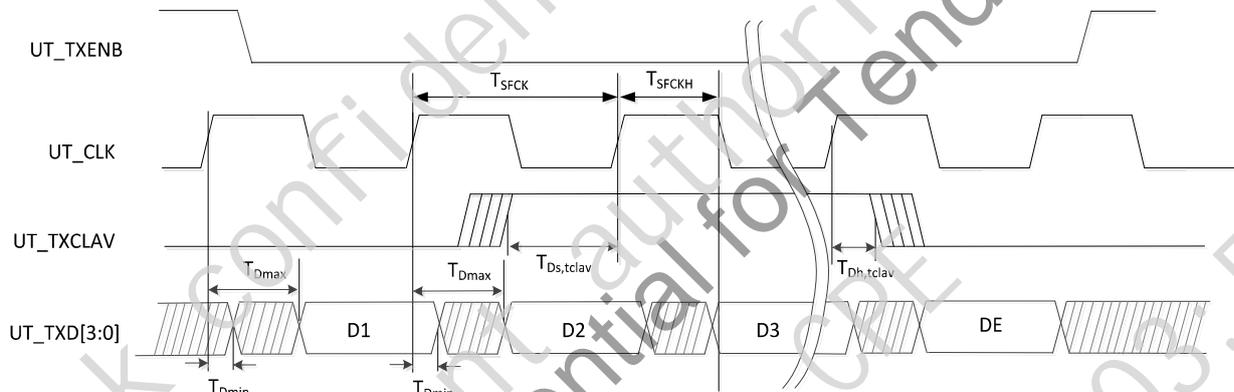
Table 30. NFBI Slave Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	NFBI MDC Period	-	40	-	ns	1
T_{CKL}	MDC High Time	-	$0.5 * T_{CK}$	-	ns	-
T_{CKH}	MDC Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{Dmax}	MDIO output max delay from MDC rising	-	-	9.3	ns	-
T_{Dmin}	MDIO output min delay from MDC rising	3.0	-	-	ns	-
T_{Ds}	MDIO input setup time to MDC rising	3.0	-	-	ns	-
T_{Dh}	MDIO input hold time from MDC rising	-0.41	-	-	ns	-

Note 1: MDC is an input signal.

11.8. VDSL PHY Bonding Interface

11.8.1. Utopia Master TX Interface Timing


Figure 26. Utopia Master TX Interface Input and Output Timing
Table 31. Utopia Master TX Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	UT_CLK Period	-	8	-	ns	125Mhz
T_{CKH}	UT_CLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
T_{Dmax}	UT_TXD[3:0], UT_TXENB output max delay from UT_CLK rising	-	-	6.6	ns	-
T_{Dmin}	UT_TXD[3:0], UT_TXENB output min delay from UT_CLK rising	2.8	-	-	ns	-
$T_{Ds,tclav}$	UT_TXCLAV input setup time to UT_CLK rising	-0.7	-	-	ns	-
$T_{Dh,tclav}$	UT_TXCLAV input hold time from UT_CLK rising	3.8	-	-	ns	-

Note 1: Typical Utopia clock is 125MHz. It is tuned in accordance with requirements.

Note 2: Input signal: UT_TXCLAV.

Note 3: Output signals: UT_CLK, UT_TXD[3:0], UT_TXENB.

11.8.2. Utopia Master RX Interface Timing

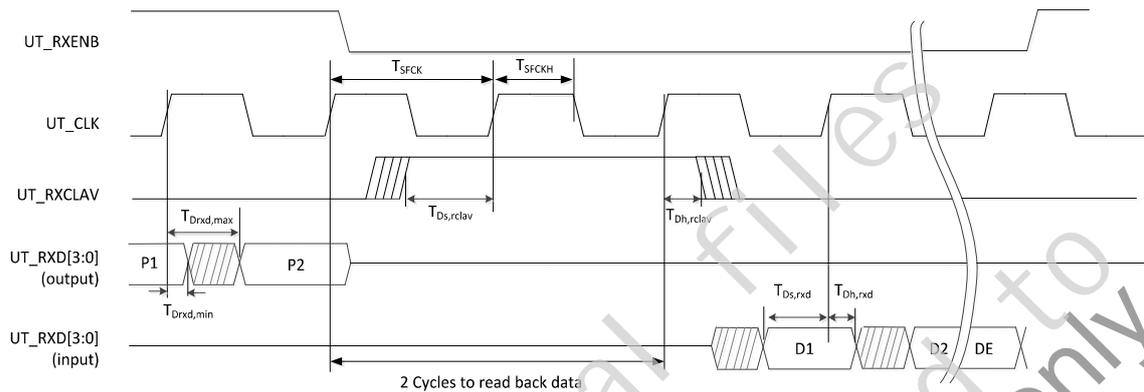


Figure 27. Utopia Master RX Interface Input and Output Timing

Table 32. Utopia Master RX Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	UT_CLK Period	-	8	-	ns	125Mhz
T_{CKH}	UT_CLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
$T_{Drxd,max}$	UT_RXD[3:0], UT_RXENB output max delay from UT_CLK rising	-	-	6.9	ns	-
$T_{Drxd,min}$	UT_RXD[3:0] UT_RXENB output min delay from UT_CLK rising	2.2	-	-	ns	-
$T_{Ds,rclav}$	UT_RXCLAV input setup time to UT_CLK rising	-0.3	-	-	ns	-
$T_{Dh,rclav}$	UT_RXCLAV input hold time from UT_CLK rising	4.2	-	-	ns	-
$T_{Ds,rxd}$	UT_RXD[3:0] input setup time to UT_CLK rising	-0.3	-	-	ns	-
$T_{Dh,rxd}$	UT_RXD[3:0] input hold time from UT_CLK rising	4.2	-	-	ns	-

Note 1: Typical Utopia clock is 125MHz. It is tuned in accordance with requirements.

Note 2: Input signal: UT_RXCLAV

Note 3: Output signals: UT_CLK, UT_RXENB

Note 4: Input/Output signals: UT_RXD[3:0]

Note 5: UT_CLK is referred by both UT_RX* and UT_TX* signals

11.8.3. Utopia Slave TX Interface Timing

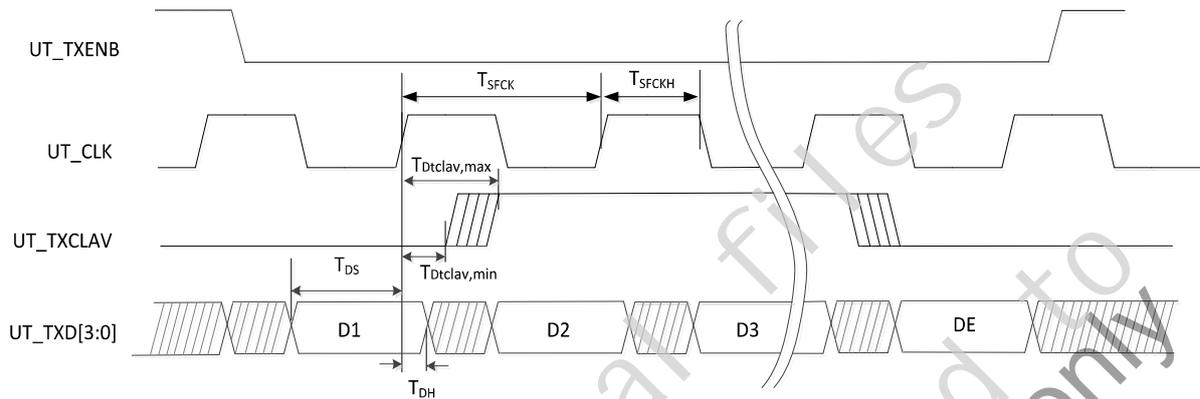


Figure 28. Utopia Slave TX Interface Input and Output Timing

Table 33. Utopia Slave TX Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	UT_CLK Period	-	8	-	ns	125Mhz
T_{CKH}	UT_CLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
$T_{Dtclav,max}$	UT_TXCLAV output max delay from UT_CLK rising	-	-	6.8	ns	-
$T_{Dtclav,min}$	UT_TXCLAV output min delay from UT_CLK rising	2.2	-	-	ns	-
T_{DS}	UT_TXD[3:0], UT_TXENB input setup time to UT_CLK rising	-0.7	-	-	ns	-
T_{DH}	UT_TXD[3:0], UT_TXENB input hold time from UT_CLK rising	3.6	-	-	ns	-

Note 1: Typical Utopia clock is 125MHz. It is tuned in accordance with requirements.

Note 2: Input signal: UT_CLK, UT_TXD[3:0], UT_TXENB

Note 3: Output signals: UT_TXCLAV.

11.8.4. Utopia Slave RX Interface Timing

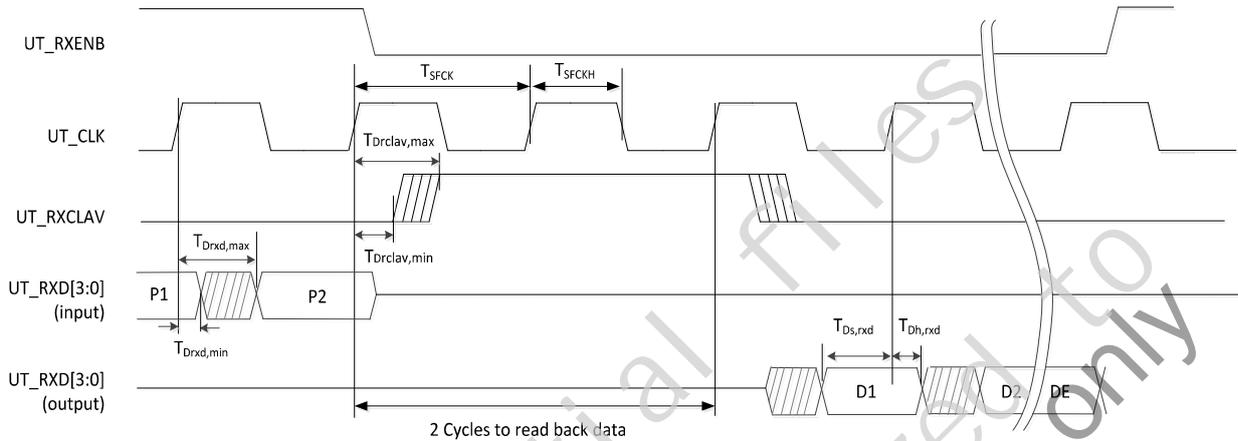


Figure 29. Utopia Slave RX Interface Input and Output Timing

Table 34. Utopia Slave RX Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T_{CK}	UT_CLK Period	-	8	-	ns	125Mhz
T_{CKH}	UT_CLK Low Time	-	$0.5 * T_{CK}$	-	ns	-
$T_{Drxd,max}$	UT_RXD[3:0] output max delay from UT_CLK rising	-	-	6.8	ns	-
$T_{Drxd,min}$	UT_RXD[3:0] output min delay from UT_CLK rising	2.1	-	-	ns	-
$T_{Drclav,max}$	UT_RXCLAV output max delay from UT_CLK rising	-	-	6.8	ns	-
$T_{Drclav,min}$	UT_RXCLAV output min delay from UT_CLK rising	2.1	-	-	ns	-
$T_{Ds,rxd}$	UT_RXD[3:0], UT_RXENB input setup time to UT_CLK rising	-0.7	-	-	ns	-
$T_{Dh,rxd}$	UT_RXD[3:0], UT_RXENB input hold time from UT_CLK rising	3.8	-	-	ns	-

Note 1: Typical Utopia clock is 125MHz. It is tuned in accordance with requirements.

Note 2: Input signal: UT_CLK, UT_RXENB

Note 3: Output signals: UT_RXCLAV

Note 4: Input/Output signals: UT_RXD[3:0]

Note 5: UT_CLK is referred to by both UT_RX* and UT_TX* signals.

11.9. Power Sequence

11.9.1. General

With regard to the power-up sequence, there is no relation between 3.3V (I/O) and 1.1V (core and analog).

The system detects voltage level over threshold and then releases. We expect stability to occur within 100ms

11.9.2. Power Up Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

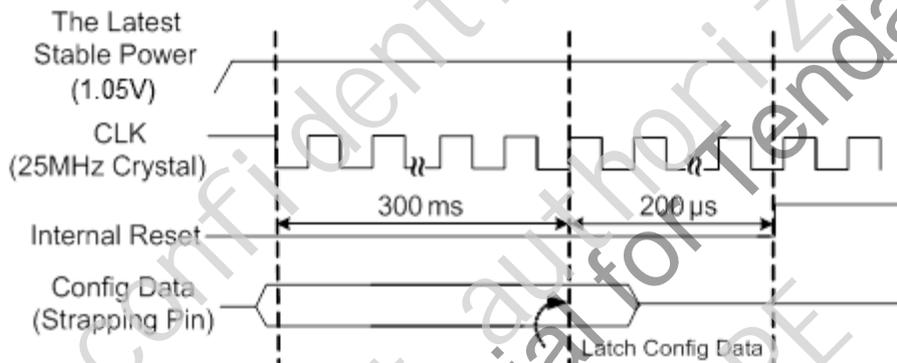
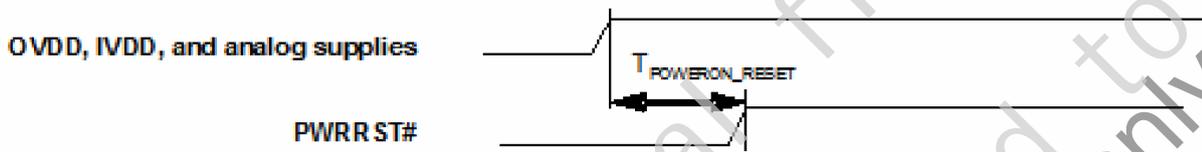


Figure 30. Power Up Configuration Timing

11.10. Reset

Table 35. Reset

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T _{poweron_reset}	Minimum time required to hold the PWRRST# at logic 0 state after stable power has been applied to RTL8685PB	-	300	-	ms	-


Figure 31. Reset Timing

11.11. VREF Timing

Table 36. VREF Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T _{delay}	Delay time from dying gasp detect to ADSL dying gasp indication bit clear	-	-	13	ns	1
T _{rp}	Required residual power sustain time	-	35	-	ms	2

Note 1: This indicates the internal delay of the chip between VREF detecting a HIGH-to-LOW edge, and the relevant digital circuit activating.

$$250 * 8 * [(B+1) * M + R] * T_p * SEQ * D / (L_p * M).$$

Note 2: To current commercial ADSL2+ systems, a minimum period of 35ms is recommended.

12. Thermal Parameters

Table 37. Assembly Descriptions for Thermal Simulation

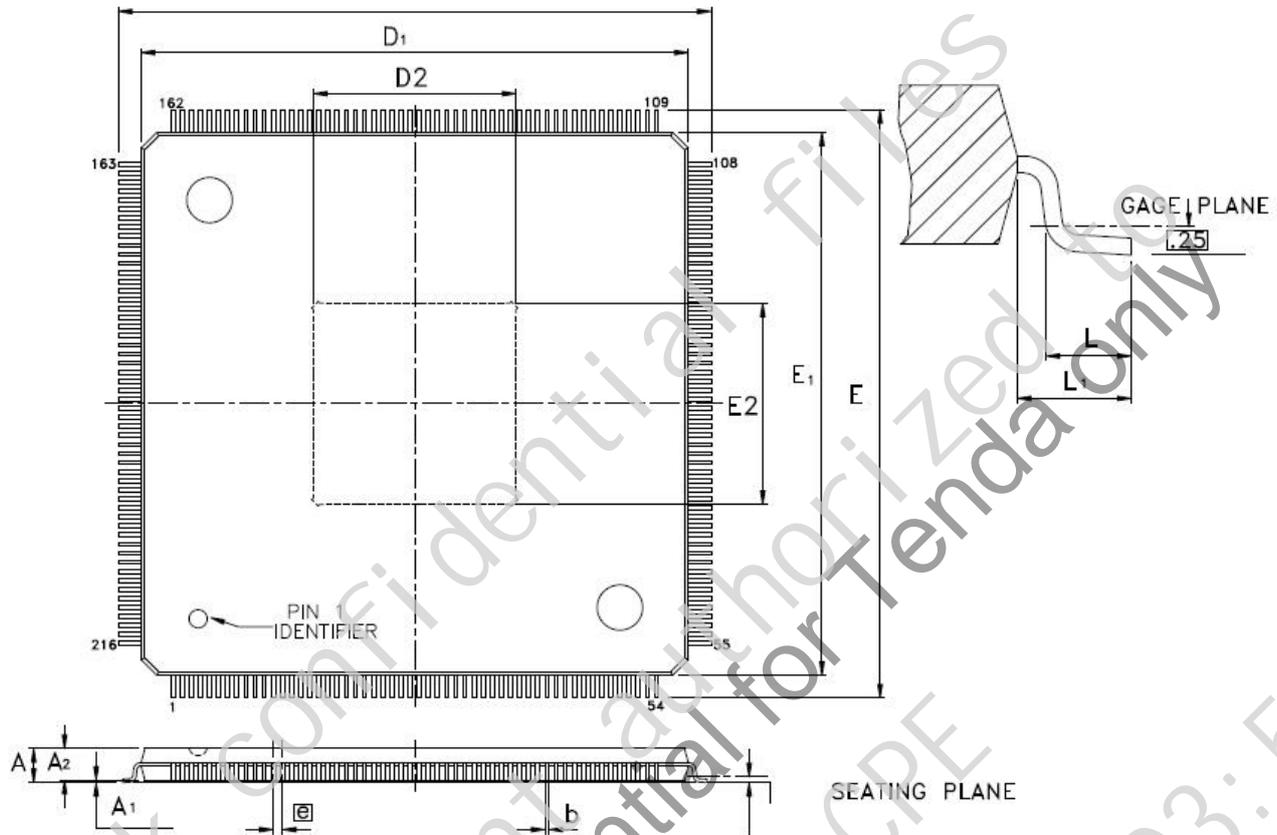
Package	Package type	LQFP
	Lead count	216L
	Package size	24 x 24 mm ²
	Compound thickness	1.6 mm
	Leadframe thickness	0.18 mm
PCB 2-Layer/ 4-Layer	PCB Dimensions (L x W)	101.6 × 114.3 mm ²
	PCB Thickness	1.6 mm
Heat sink	Dimensions(L x W x H)	35 x 35 x 10 mm ³

Table 38. Thermal Performance

Heat Sink	PCB Layer	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	ψ_{Jt} (°C/W)
With	2L	20.85	-	-	7.83
	4L	18.83	-	-	6.70
Without	2L	26.30	18.50	10.90	0.81
	4L	22.41	14.48	9.69	0.69

Note: Power consumption is detailed in section 10.3 Total Power Consumption, page 29.

13. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
D/E	26.00 BSC			1.024 BSC		
D1/E1	24.00 BSC			0.945 BSC		
D2/E2	6.88	7.01	7.14	0.271	0.276	0.281
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes:

CONTROLLING DIMENSION: MILLIMETER (mm).

REFERENCE DOCUMENT: JEDEC MS-026.

14. Ordering Information

Table 39. Ordering Information

Part Number	Package	Description	Status
RTL8685PB-VB6-CG	LQFP-216E	VDSL 35b SoC with 1GHz CPU and 256Mbyte DRAM embedded, bonding capable	MP
RTL8685PB-VA5-CG	LQFP-216E	VDSL 35b SoC with 1GHz CPU and 128Mbyte DRAM embedded	MP
RTL8685PB-VB5-CG	LQFP-216E	VDSL 35b SoC with 1GHz CPU and 128Mbyte DRAM embedded, bonding capable	MP
RTL8685PB-VF5-CG	LQFP-216E	VDSL 35b SoC 750MHz CPU and 128Mbyte DRAM embedded	MP
RTL8685PB-VL5-CG	LQFP-216E	VDSL 30a SoC 750MHz CPU with 128Mbyte DRAM embedded	MP
RTL8685PB-VL4-CG	LQFP-216E	VDSL 30a SoC 750MHz CPU with 64Mbyte DRAM embedded	MP
RTL8685PB-VL3-CG	LQFP-216E	VDSL 35B SoC 750MHz CPU with 32Mbyte DRAM embedded, bonding capable	MP

Note: See page 11 for package identification information.

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